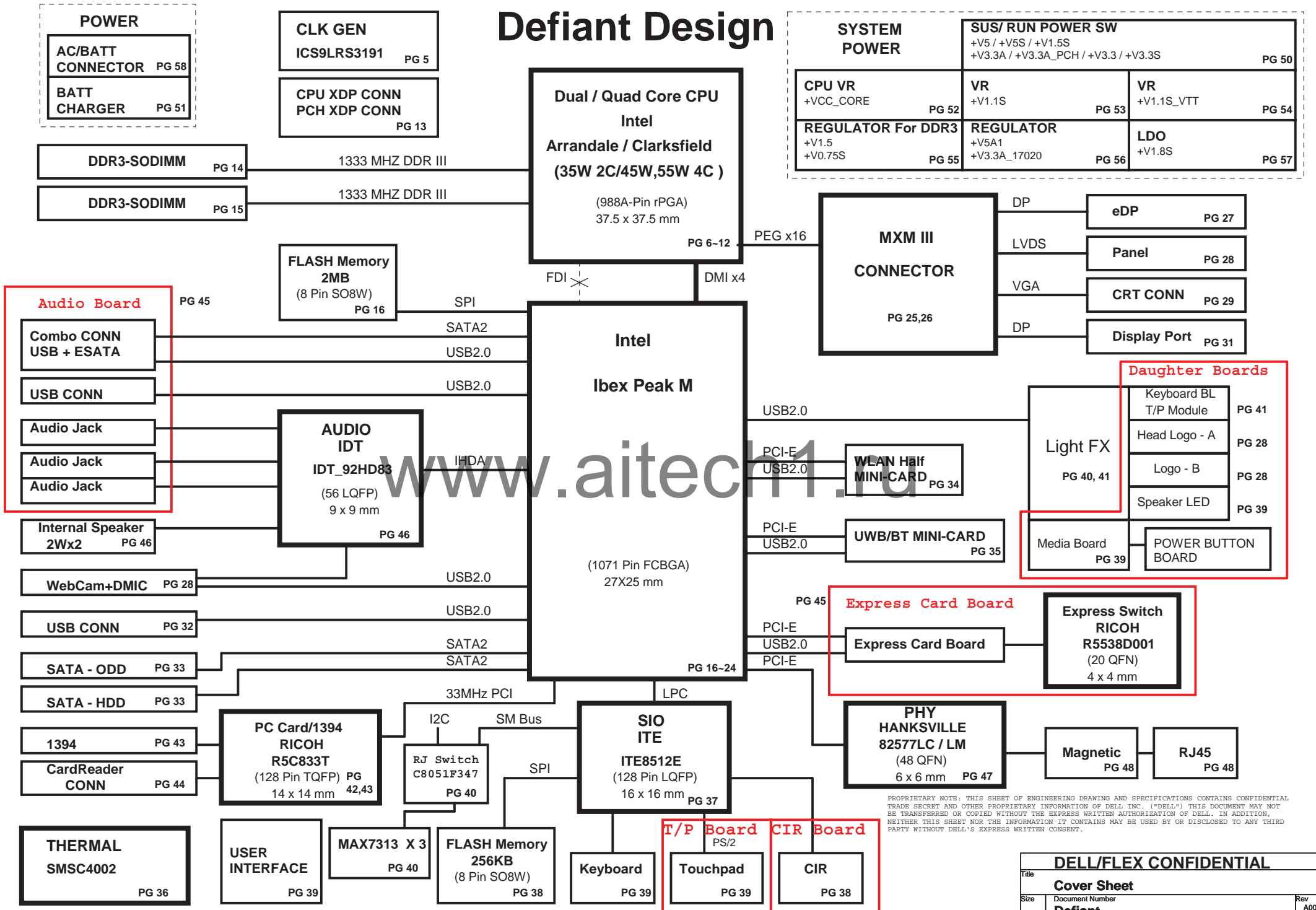


Defiant Design



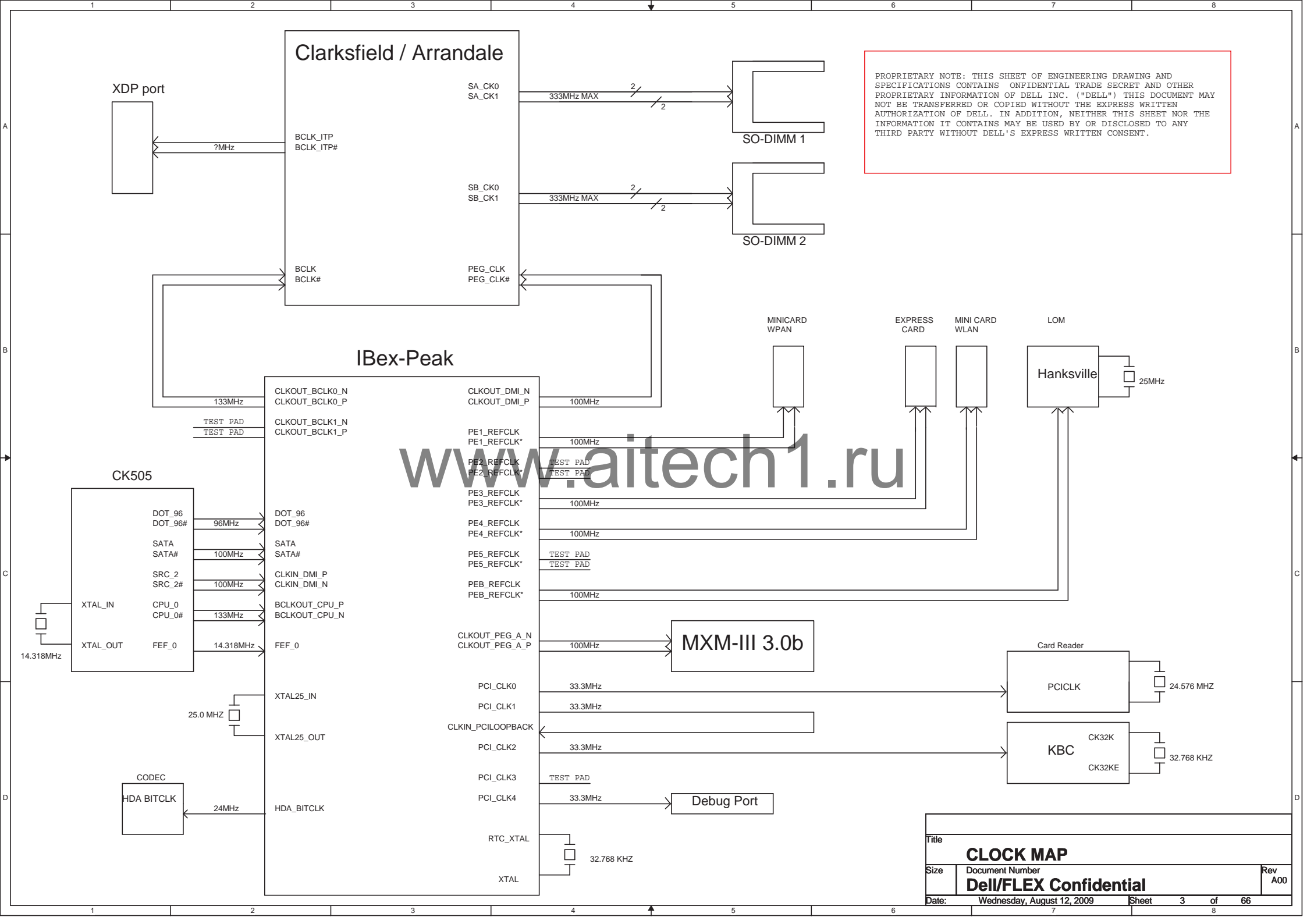
INDEX		INDEX	
Page#	Description	Page#	Description
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2	Front Page	44	CardReader CONN
3	CLOCK MAP	45	Audio Board and Exp Board CONN
4	POWER SEQUENCING	46	Audio_(92HD83)/CON
5	CLOCK GEN (SLG8SP585)	47,48	PHY(HANKSVILLE),RJ45&Transform
6-12	CPU (Arrandale / Clarksfield)	49	System Reset Circuit
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14,15	DDRIII SO-DIMM(204P)	51	CHARGER (MAX8731)
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25,26	MXM CONN	53	+V1.1S (MAX8792)
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28	LCD Conn	55	DDR3 1.5V/0.75V (MAX8632)
29	CRT Conn	56	SYS 5V/3V(MAX17020)
30	MXM& PCH DDC/ AUX MUX	57	+V1.8S (RT9025-25PSP)
31	DP CONN	58	DCIN Bait
32	USB	59	PAD/ SCREW/ Moat Cap
33	HDD & CD ROM/ G-Sensor	60	Power Block Diagram
34	MINI-CARD (WLAN)	61	Reset Map
35	MINI-CARD (WPAN)	62	LED BOARD
36	FAN & THERMAL EMC4002	63	KBC Power Up Sequence
37	SIO (ITE8512)	64	SMBus Map_PCH
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39	Keyboard, Daughtor Board conn & User Interface	66-67	HISTORY
40,41	LED Light FX		

Power States								
Power Rail	Control Signal	S0	S3	S4	S5	G3	S4/ M-off	S5/ M-off
+PWR_SRC	N/A	V	V	V	V			
+V0.75S	RUN_ON	V						
+V1.1S_VTT	+V1.1S_VTT_MXM1_PWRON	V						
+V1.1S	RUN_ON	V						
+V1.5S	RUN_ON	V						
+V1.5	SUS_ON	V	V					
+V1.8S	RUN_ON	V						
+V3.3A	3V_ALW_ON	V	V	V	V			
+V3.3M_LAN	PM_SLP_LAN#	V	define WOL	define WOL	define WOL			
+V3.3S	RUN_ON	V						
+V3.3	SUS_ON	V	V					
+V5A1	+5V_EN2	V	V	V	V			
+V5A2	+PWR_SRC	V	V	V	V			
+V5	SUS_ON	V	V					
+5V_HDD	N/A	V						
+5V_MOD	N/A	V						
+V5S	RUN_ON	V						
+GFX_PWR_SRC	RUN_ON	V						
+LCDVCC	ENVDD	V						
+V3.3A_RTC	RTC	V	V	V	V	V		
+VCC_CORE	IMVP_VR_ON	V						
+USB_RIGHT_PWR	USB_SIDE_EN#	V	define	define				
+USB_LEFT_PWR	USB_BACK_EN#	V	define					
+V15_A	N/A	V	V	V	V			
+V3.3A_17020	+3.3V_EN2	V	V	V	V			
+V1.0M_LAN	PM_SLP_LAN#	V	define WOL	define WOL	define WOL			

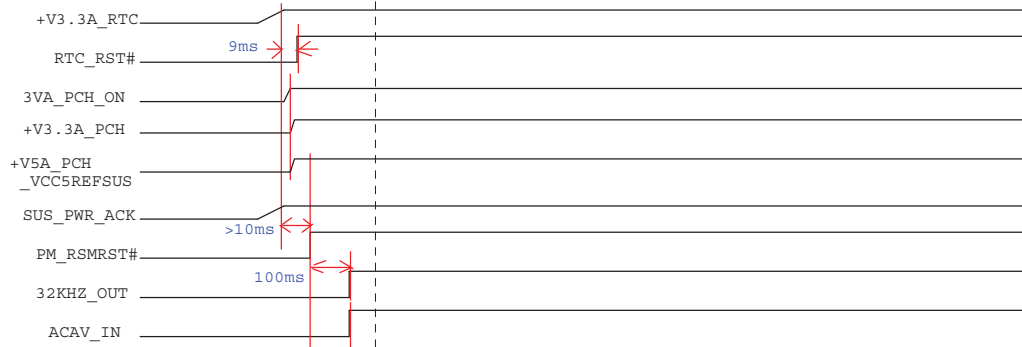
By Albert

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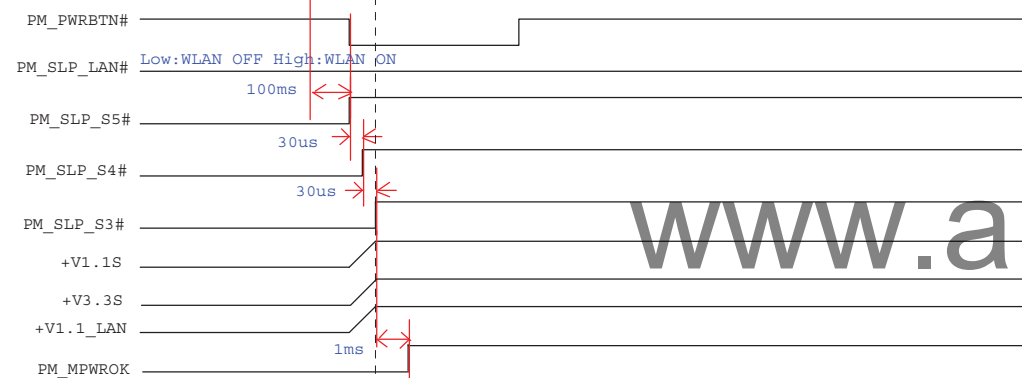
Title			
FRONTPAGE			
Size	Document Number		Rev
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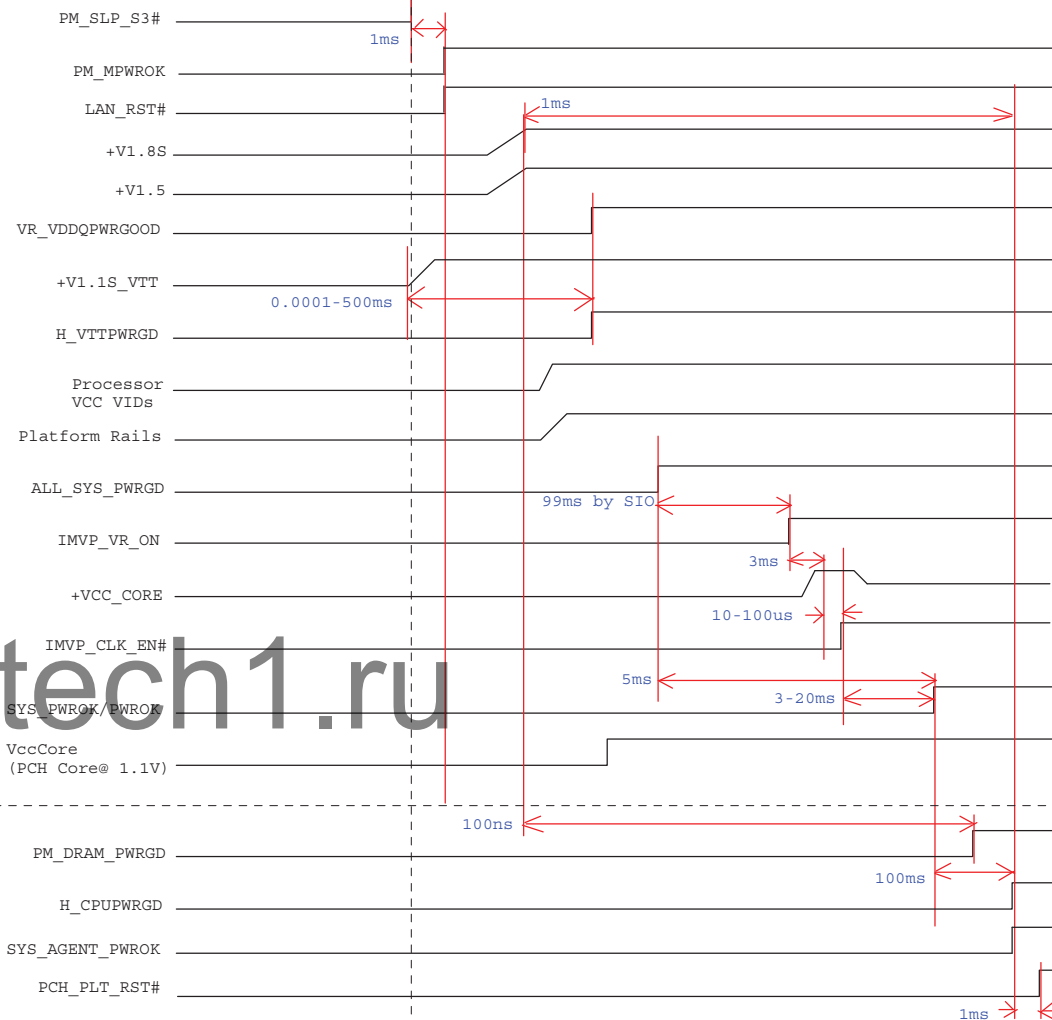
G3 to Sx



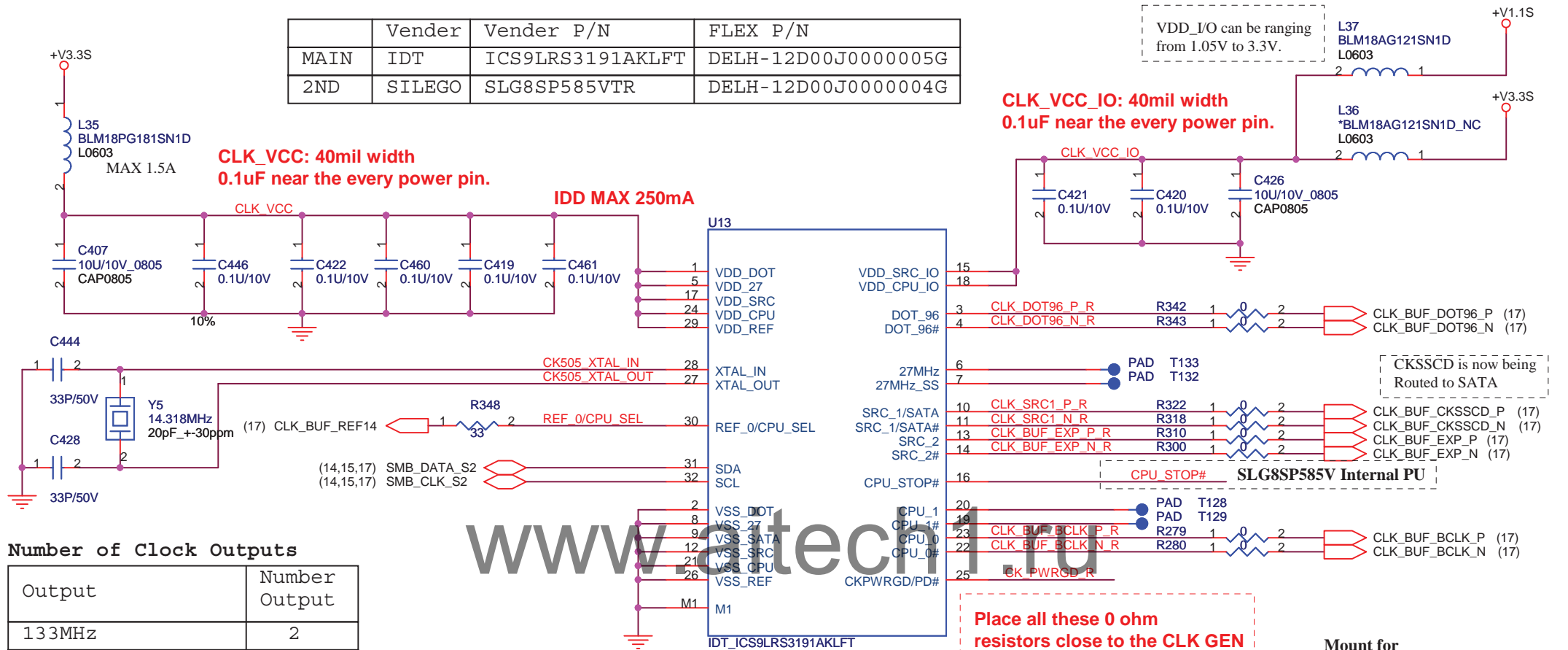
Sx to S0



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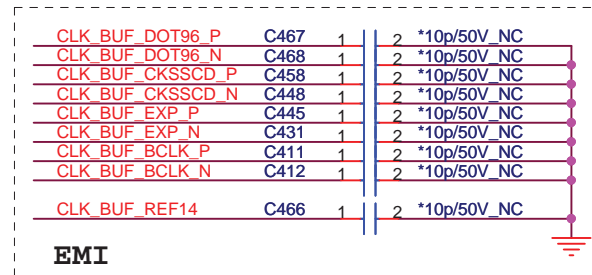


	Vender	Vender P/N	FLEX P/N
MAIN	IDT	ICS9LRS3191AKLFT	DELH-12D00J00000005G
2ND	SILEGO	SLG8SP585VTR	DELH-12D00J00000004G



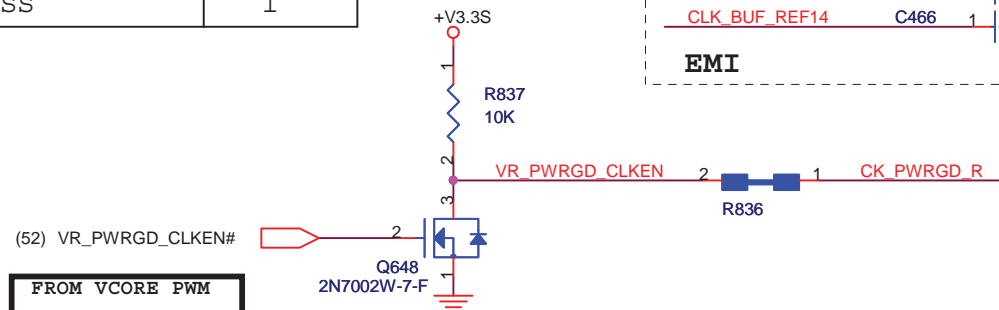
Number of Clock Outputs

Output	Number Output
133MHz	2
SRC(100MHz_SS)	1
SRC/SATA (100MHz)	1
USB (48MHz)	1
REF (14.3181MHz)	1
DOT_CLK (96MHz)	1
27MHz	1
27MHz SS	1



CPU_SEL During CK_PWRGD Latch Pin 30

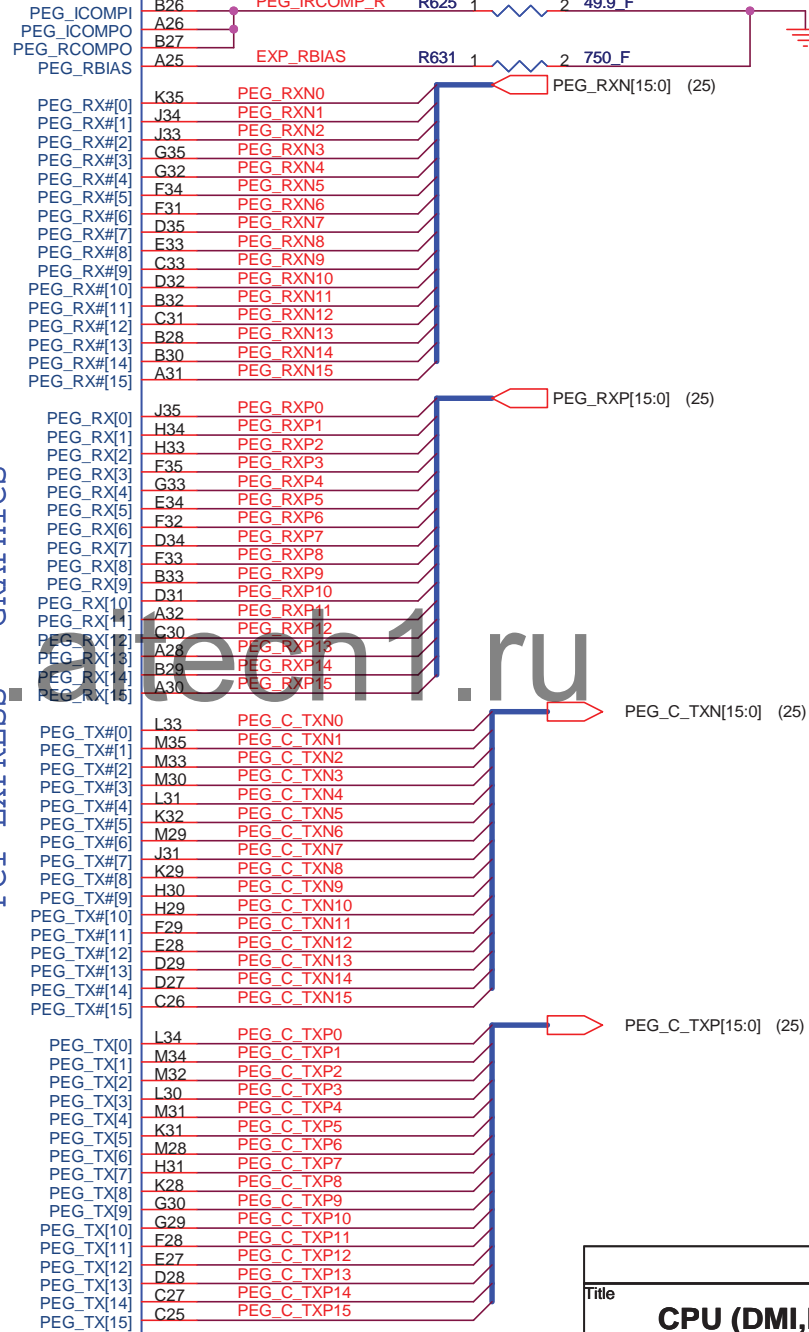
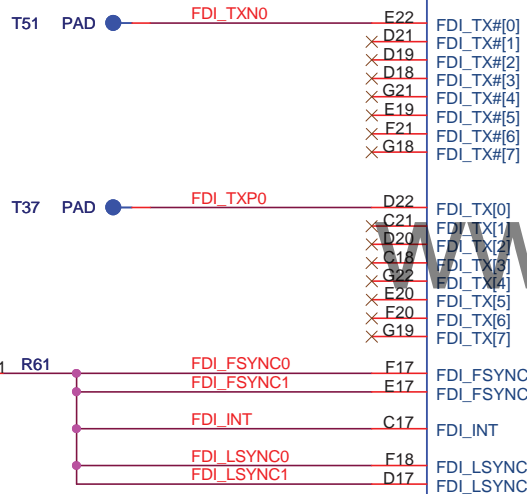
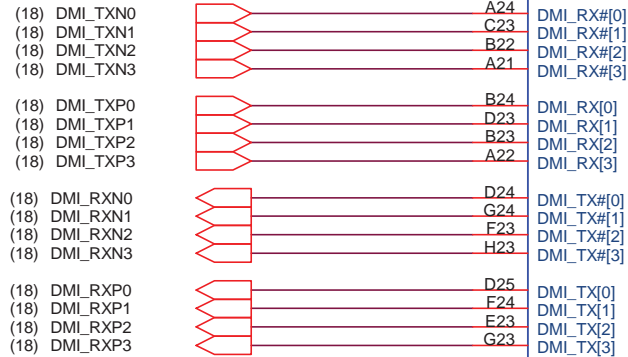
Input (pin 30)	CPU_0/_1	SRC
0 -> NOW	133MHz	100MHz
1	100MHz	100MHz



Title		
CLOCK GEN (ICS9LRS3191)		
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ARRANDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)

U600A



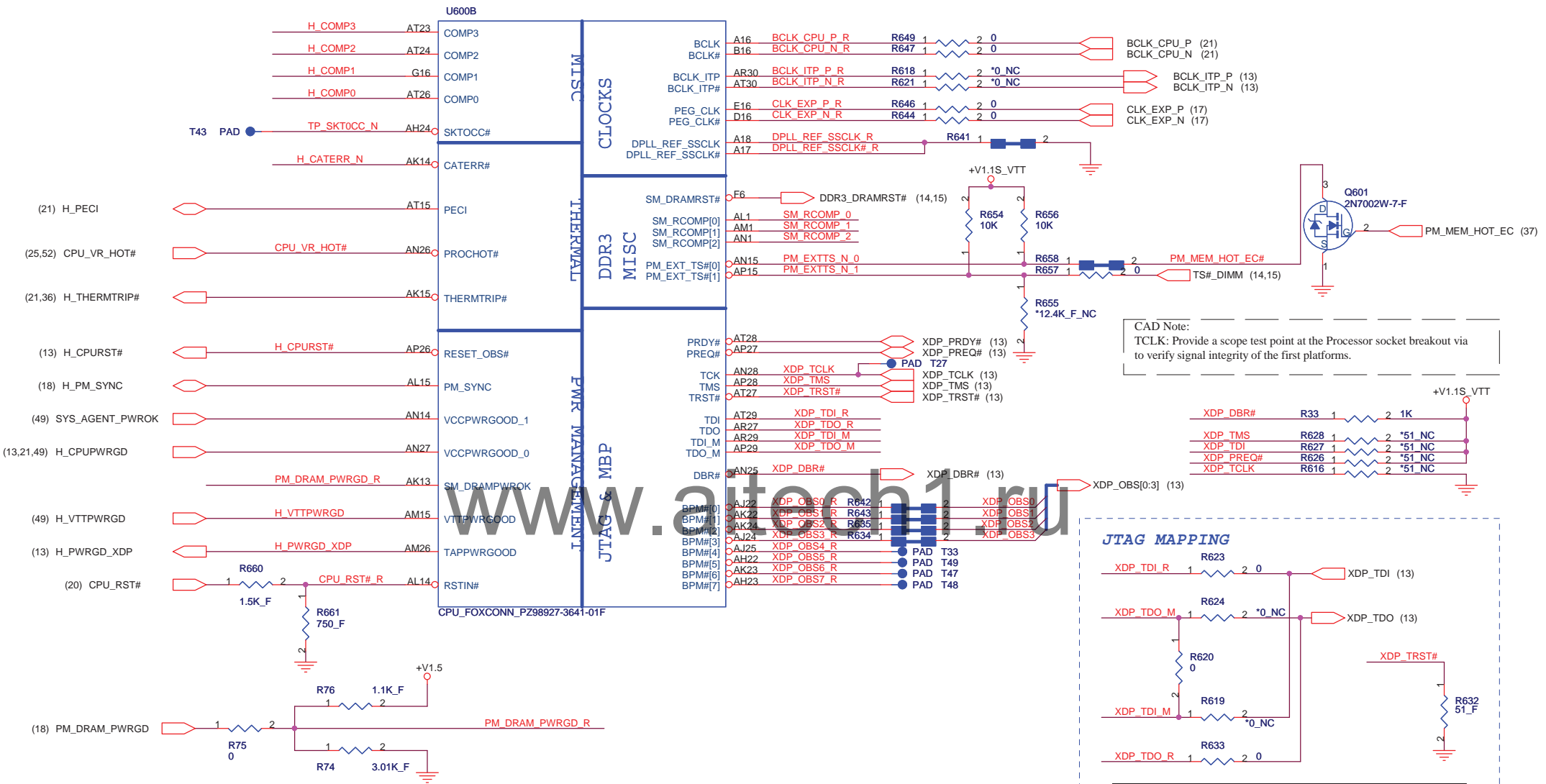
CPU Socket	FLEX P/N
FOXCONN	DELH-39D0120000003G
TYCO	DELH-39D0120000006G
Lotes	DELH-39D0120000007G

CLARKSFIELD CPU	FLEX P/N
45W 1G6 i7-720QM	DELH-11D00100000032G
45W 1G73 i7-820QM	DELH-11D00100000033G
55W 2G i7-920XM	DELH-11D00100000034G

CPU_FOXCONN_PZ98927-3641-01F

Title		
CPU (DMI,PEG,FDI) 1/7		
Size	Document Number	Rev
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ARRANDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)



Processor Pullups

+V1.1S_VTT

R63 49.9_F

R48 68

R47 *68_NC

H_CATERR_N

CPU_VR_HOT#

H_CPURST#

Processor Compensation Signals

H_COMP0

H_COMP1

H_COMP2

H_COMP3

R636 49.9_F

R54 49.9_F

R639 20_F 0402

R640 20_F 0402

DDR3 Compensation Signals

SM_RCOMP_2

SM_RCOMP_1

SM_RCOMP_0

Layout Note:
Place these resistors near Processor

R82 100_F

R81 24.9_F

R80 130_F

Scan Chain (Default)

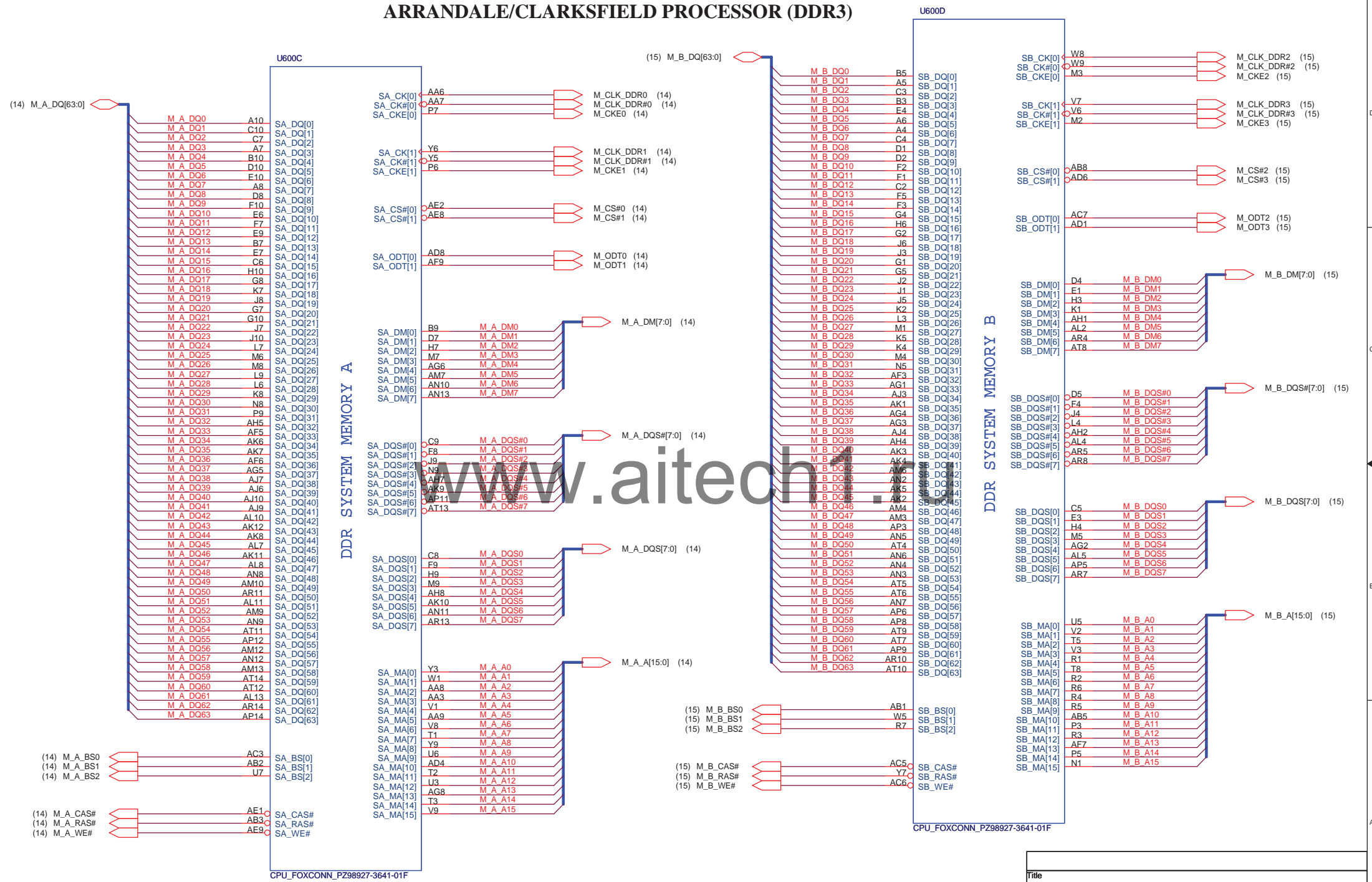
CPU Only	
GMCH Only	

Title
CPU(CLK,MISC) 2/7

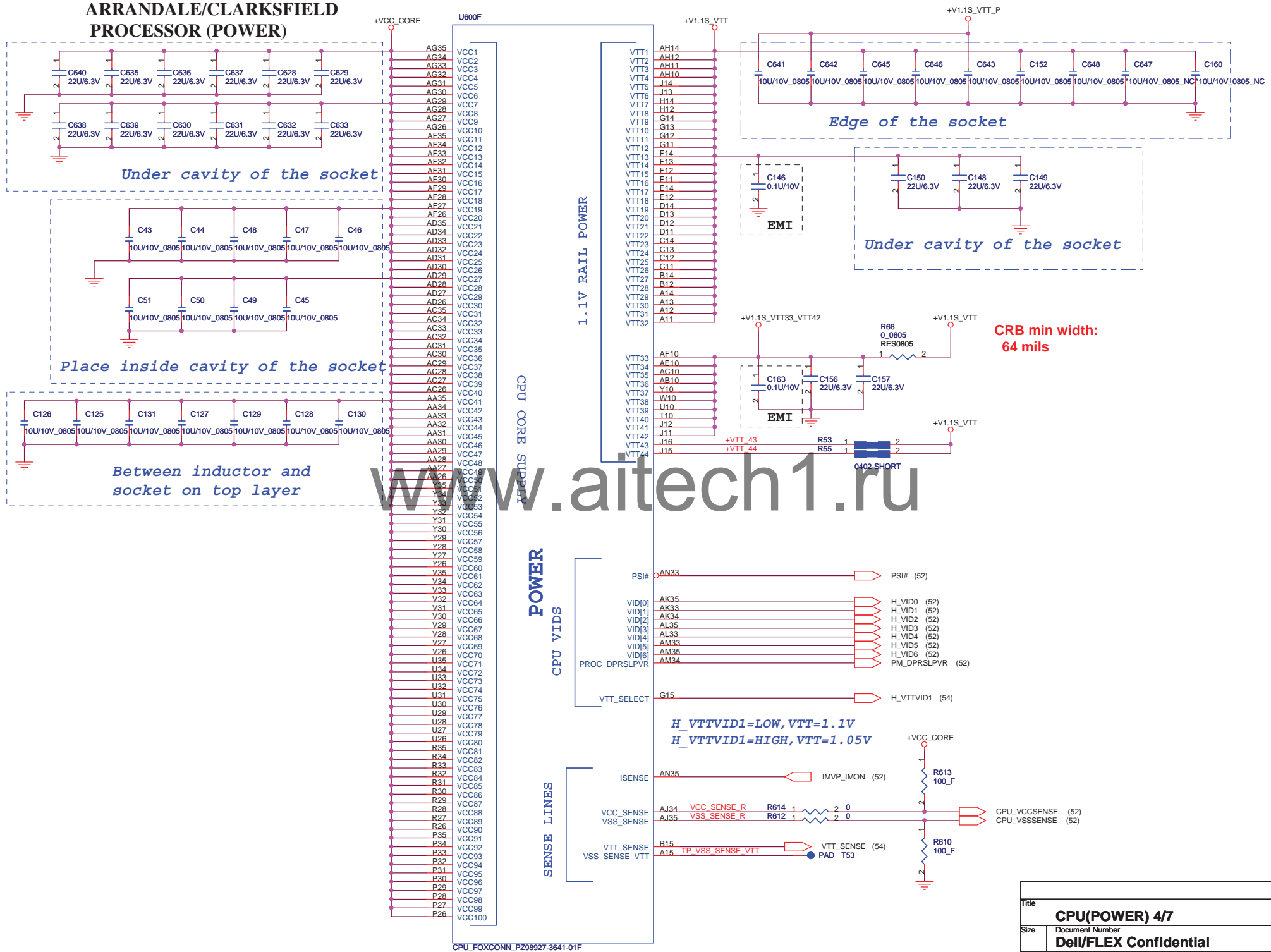
Size **Document Number**
Dell/FLEX Confidential

Date: **Wednesday, August 12, 2009** **Sheet** **7** **of** **66** **Rev** **A00**

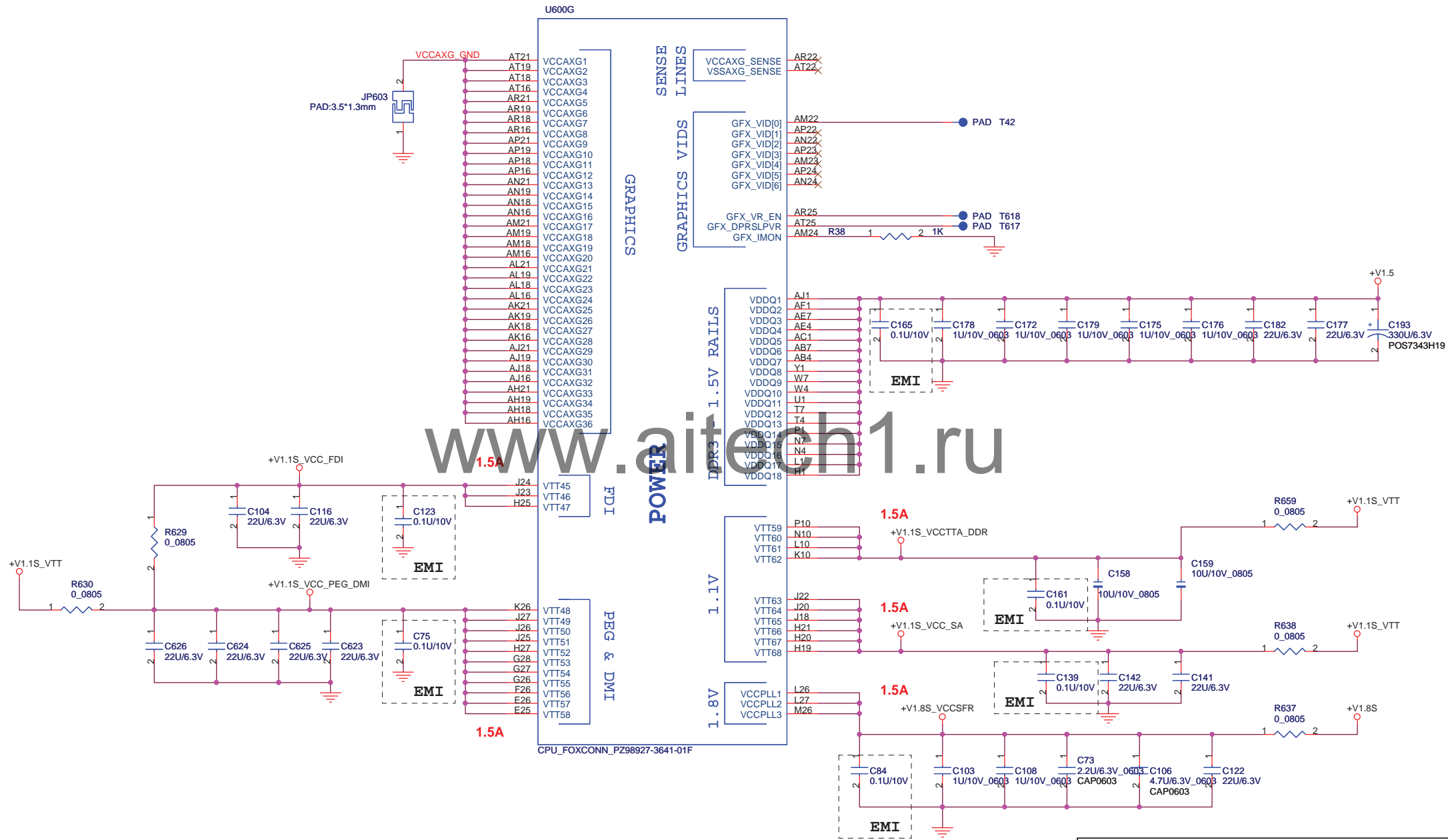
ARRANDALE/CLARKSFIELD PROCESSOR (DDR3)



ARRANDALE/CLARKSFIELD PROCESSOR (POWER)

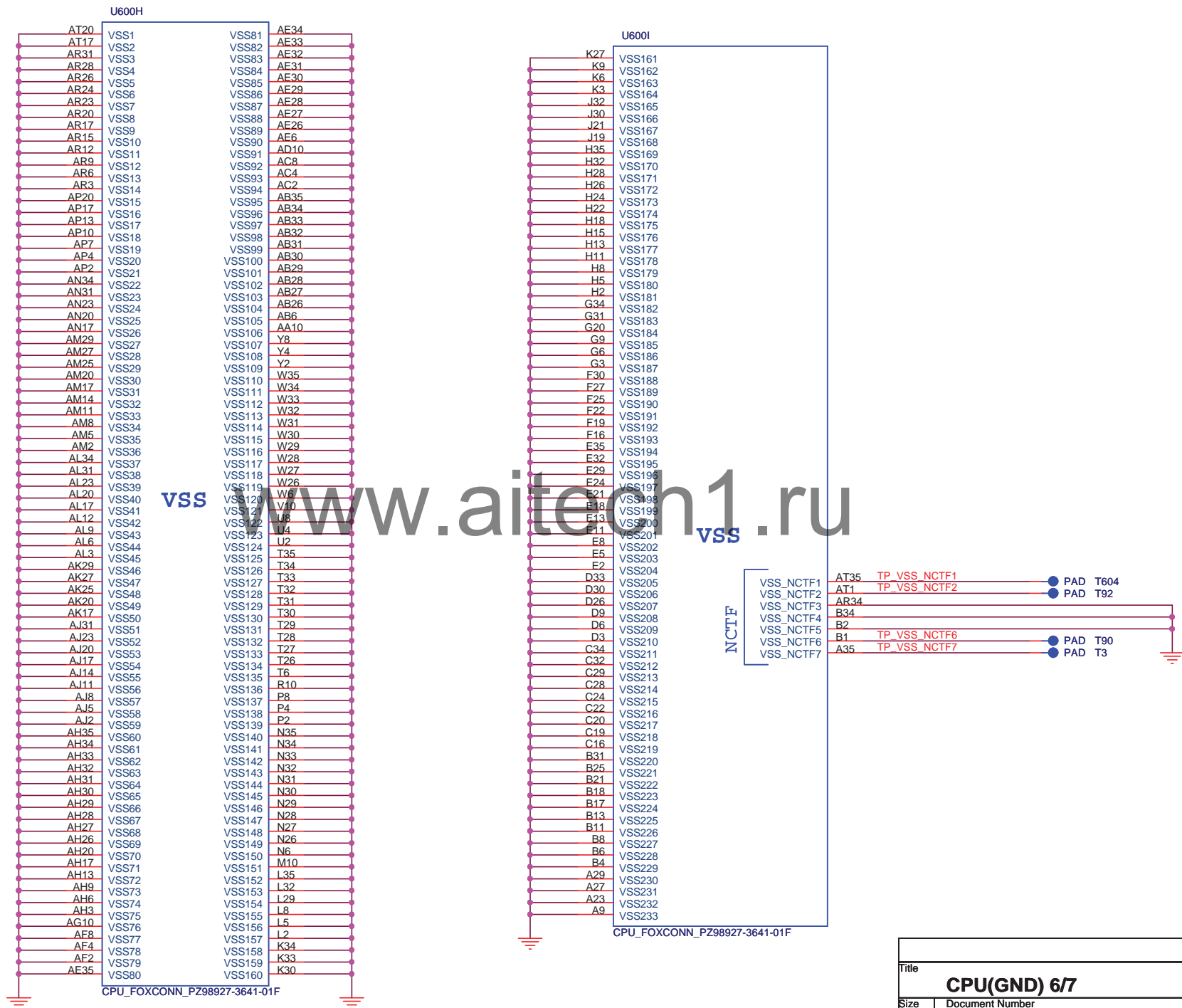


ARRANDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)



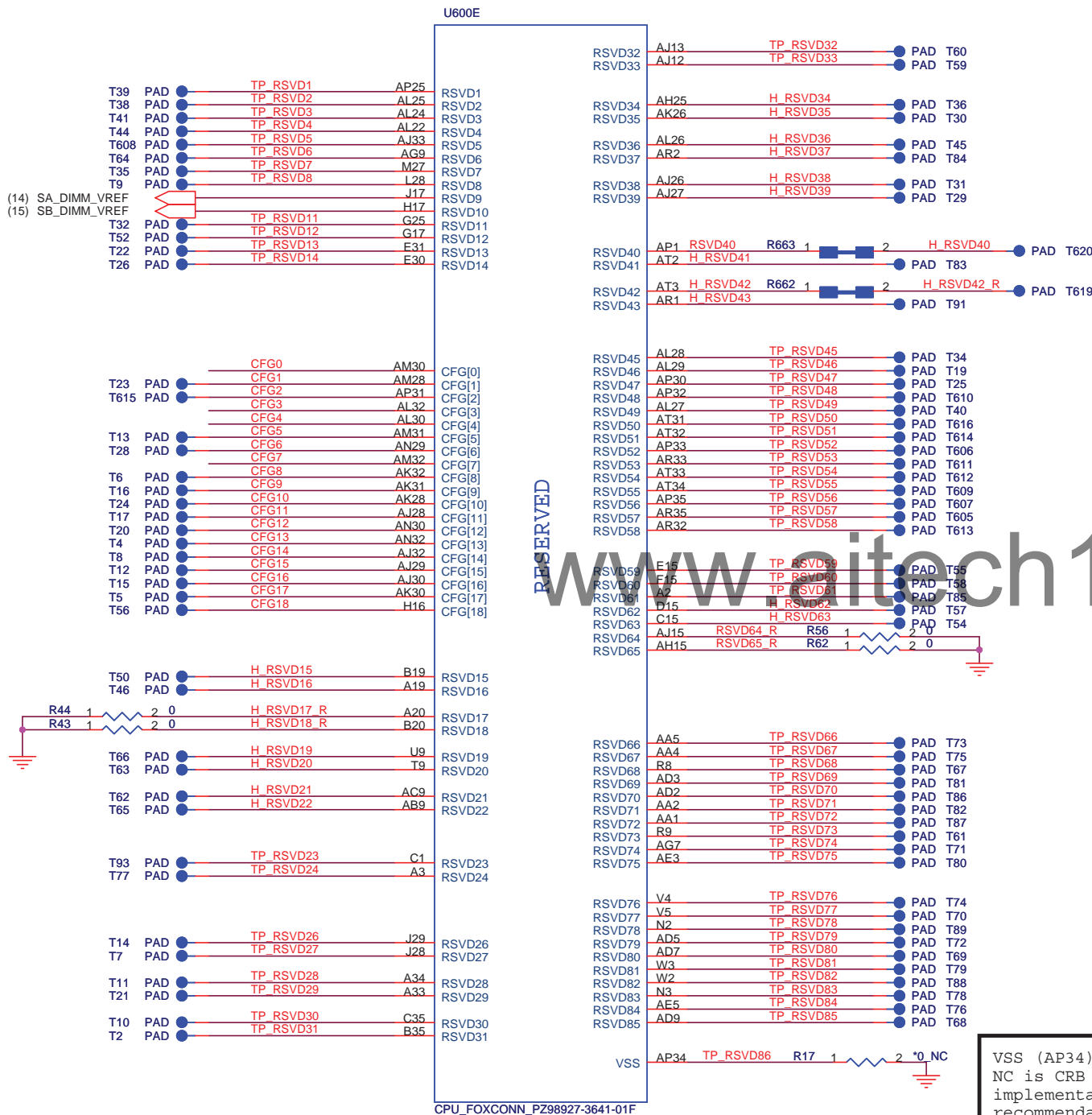
Title				
CPU(GRAPHICS PWR) 5/7				
Size	Document Number			Rev
Dell/FLEX Confidential				A00
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ARRANDALE/CLARKSFIELD PROCESSOR (GND)



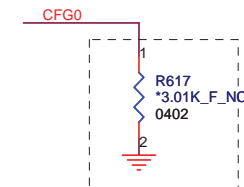
Title				
CPU(GND) 6/7				
Size	Document Number			Rev
	Dell/FLEX Confidential			A00
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ARRANDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)

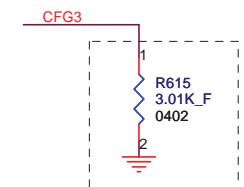


CFG Straps for PROCESSOR

PCI-Express Configuration Select	
CFG0	1:Single PEG(Default) 0:Bifurcation enabled



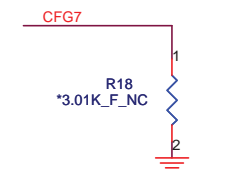
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation(Default) 0 :Lane Numbers Reversed 15 > 0, 14 > 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port (Default) 0:Enabled; An external Display Port device is connected to the Embedded Display Port

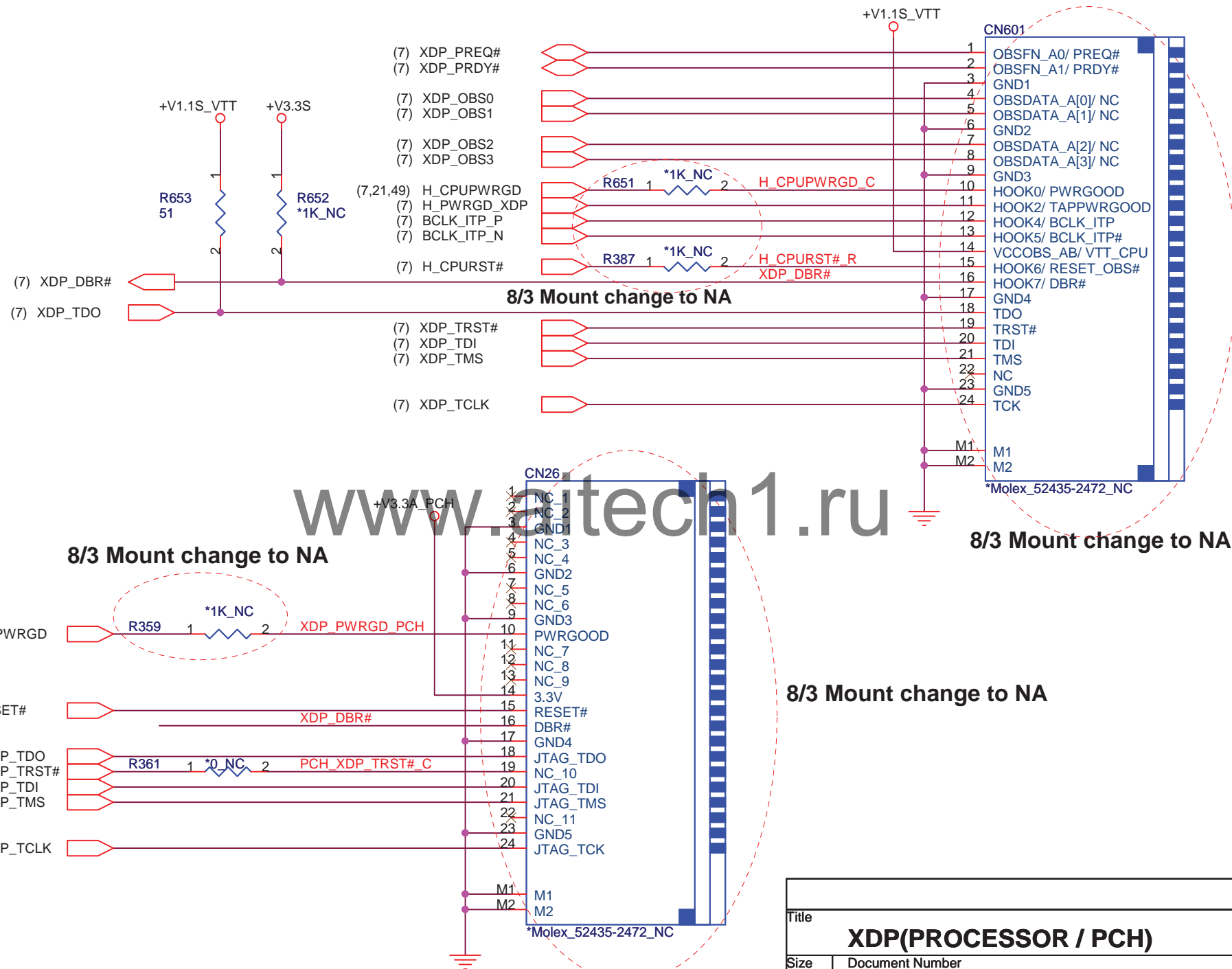


CFG7	
CFG7	Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report].

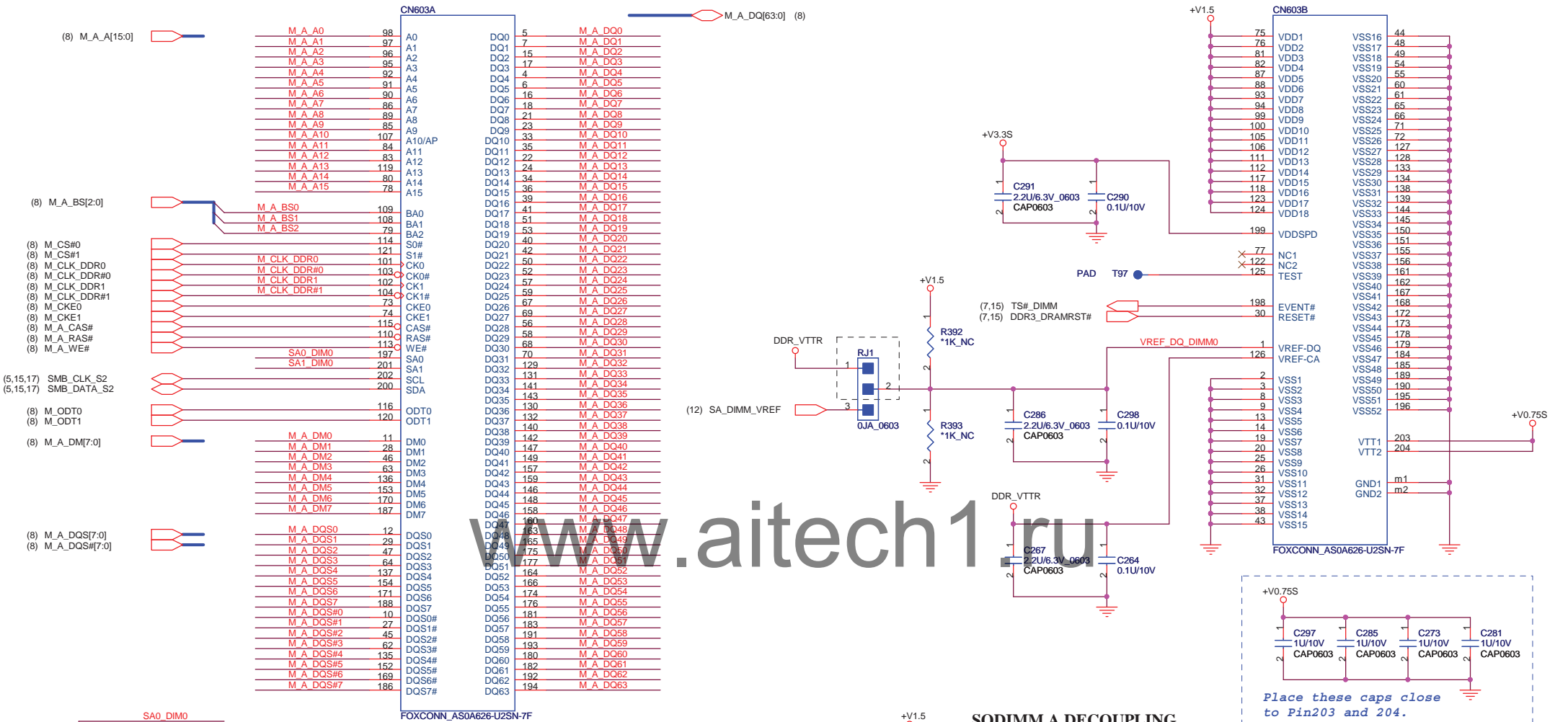


VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND

Title		
CPU(RSVD,CFG) 7/7		
Size	Document Number	Rev
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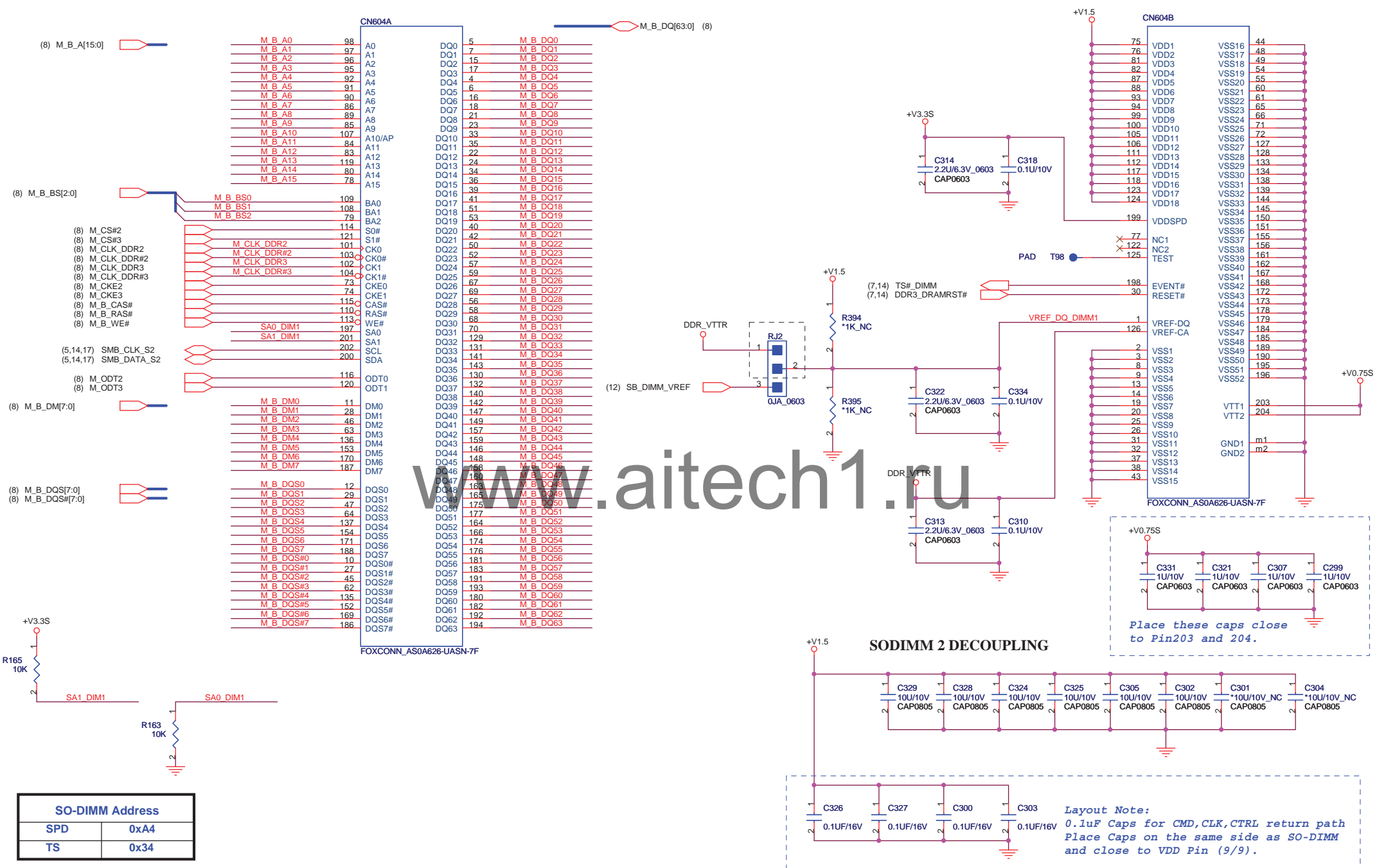
Title		
XDP(PROCESSOR / PCH)		
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SO-DIMM Address		
SA0_DIM0 = 0, SA1_DIM0 = 0	SPD	0xA0
	TS	0x30
SA0_DIM0 = 1, SA1_DIM0 = 0	SPD	0xA2
	TS	0x32

	Vender	FLEX P/N	DESCRIPTION
MAIN	FOXCONN	DELH-39D0370000009G	DDR3 SO-DIMM H:5.2mm AS0A626-U2SN-7F
2ND	TYCO	DELH-39D03700000011G	DDR3 SO-DIMM H:5.2mm 2-2013289-2

Title		DDR3 SO-DIMM1(204P)
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SO-DIMM Address	
SPD	0xA4
TS	0x34

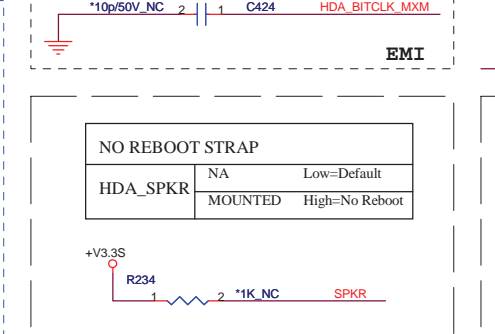
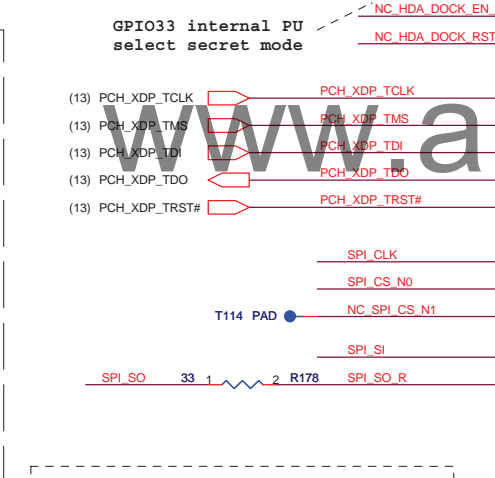
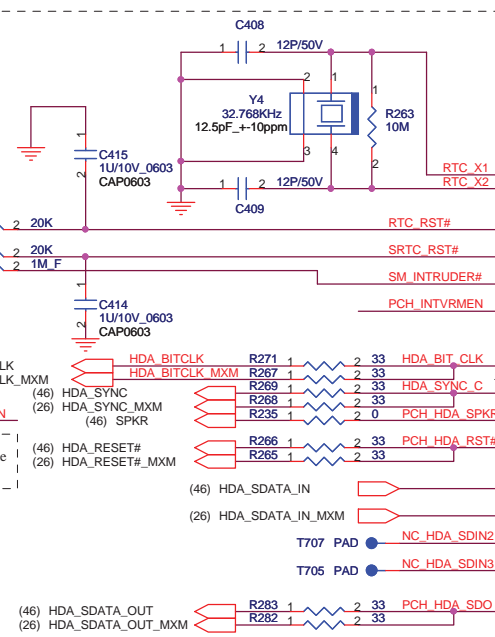
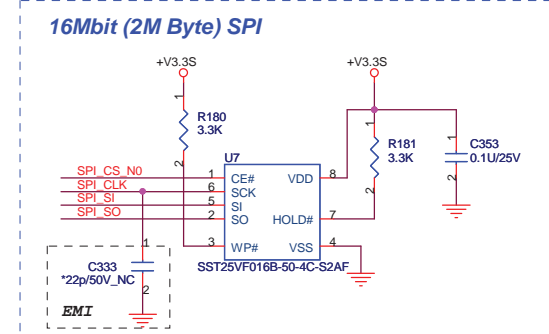
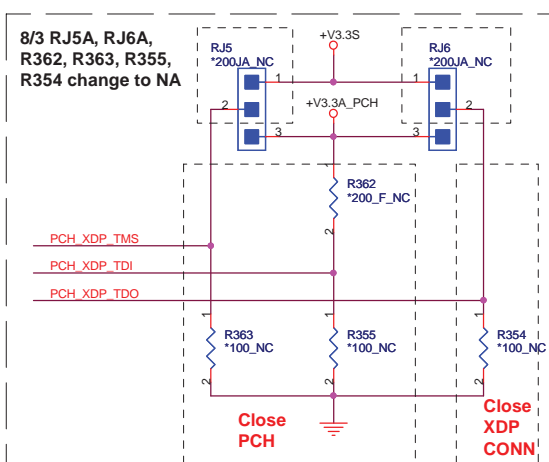
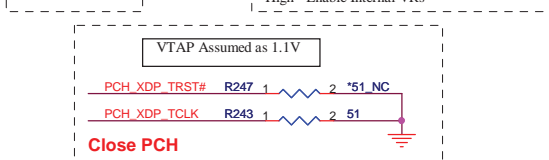
	Vender	FLEX P/N	DESCRIPTION
MAIN	FOXCONN	DELH-39D0370000010G	DDR3 SO-DIMM H:9.2mm AS0A626-UASN-7F
2ND	TYCO	DELH-39D0370000012G	DDR3 SO-DIMM H:9.2mm 2-2013310-2

Title DDR3 SO-DIMM2(204P)		
Size	Document Number Deil/FLEX Confidential	Rev A00
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The schematic diagram illustrates the connection between the BT600 module, the RTC, and the battery (BAT). The BT600 module is connected to the RTC through a network of resistors (R292, R290, R303, R305) and capacitors (C676, CAP0603). The BAT is connected to the RTC through a network of resistors (R689, R305) and capacitors (C676, CAP0603). The RTC is connected to the BAT through a network of resistors (R292, R290, R303, R305) and capacitors (C676, CAP0603). The BAT is connected to the RTC through a network of resistors (R689, R305) and capacitors (C676, CAP0603).

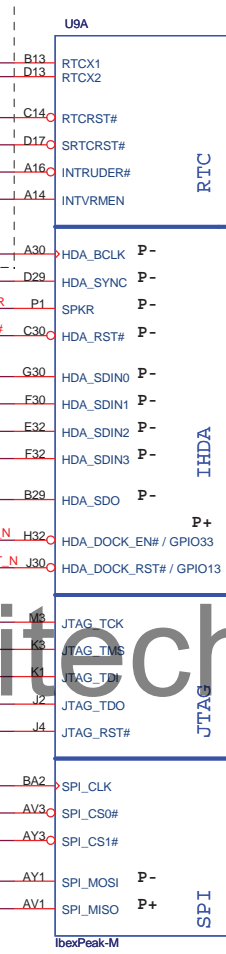
Key components and connections include:

- BT600 Module:** PWR, GND0, M1, M2, GND1.
- RTC:** RTC, BAT Conn.
- BAT:** BAT, BAT D, BAT.
- Resistors:** R292, R290, R303, R305, R689 (1K).
- Capacitors:** C676 (1u/10V_0603), CAP0603.
- Diodes:** D605, BAT54C.
- Other Labels:** +V3.3A, +V3.3A_RTC, PCH_INTVTRMEN, HDA_BITCLK, HDA_BITCLK.



U9A			
B13	RTCX1	RTC	
D13	RTCX2		
C14	RTCRST#		
D17	SRTRCST#		
A16	INTRUDER#		
A14	INTVRMEN		
A30	HDA_BCLK	P-	IHDA
D29	HDA_SYNC	P-	
P1	SPKR	P-	
C30	HDA_RST#	P-	
G30	HDA_SDINO	P-	
F30	HDA_SDIN1	P-	
E32	HDA_SDIN2	P-	
F32	HDA_SDIN3	P-	
B29	HDA_SDO	P-	
N H32	HDA_DOCK_EN# / GPIO33	P+	
N J30	HDA_DOCK_RST# / GPIO13		
M3	JTAG_TCK		JTAG
K3	JTAG_TMS		
K1	JTAG_TDI		
J2	JTAG_TDO		
J4	JTAG_RST#		
BA2	SPI_CLK		SPI
AV3	SPI_CS0#		
AY3	SPI_CS1#		
AY1	SPI_MOSI	P-	
AV1	SPI_MISO	P+	

IbexPeak-M



P+ FWH0 / LAD0 D33
P+ FWH1 / LAD1 B33
P+ FWH2 / LAD2 C32
P+ FWH3 / LAD3 A32

 FWH4 / LFRAME# C34

P+ LDRQ0# A34
 LDRQ1# / GPIO23 F34 PCH_DRQ#1

P+ SERIRQ AB9

 SATA0RXN AK7
 SATA0RXP AK6
 SATA0TXN AK11
 SATA0TXP AK9

 SATA1RXN AH6
 SATA1RXP AH5
 SATA1TXN AH9
 SATA1TXP AH8

 SATA2RXN AF11 SATA RXN2 C
 SATA2RXP AF9 SATA RXP2 C
 SATA2TXN AF7 SATA TXN2 C
 SATA2TXP AF6 SATA TXP2 C

 SATA3RXN AH3 NC SATA RXN3
 SATA3RXP AH1 NC SATA RXP3
 SATA3TXN AF1 NC SATA TXN3
 SATA3TXP AF1 NC SATA TXP3

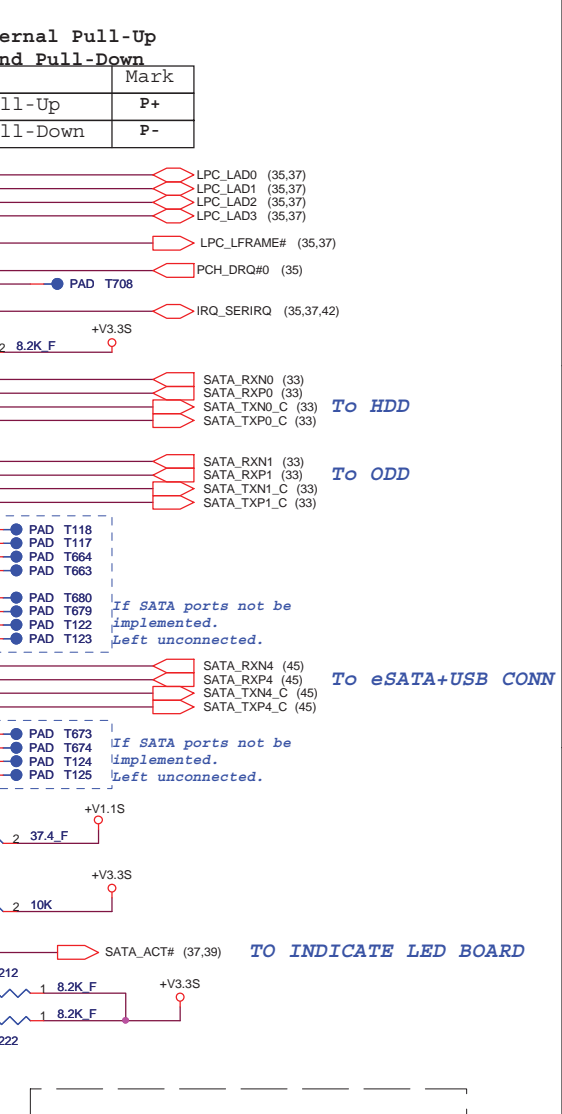
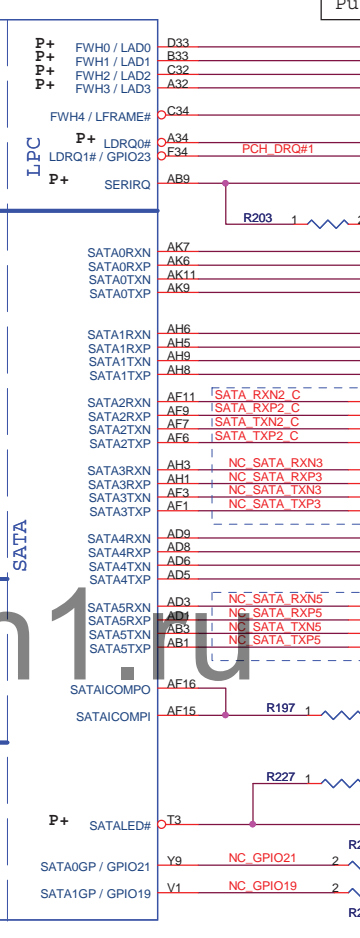
 SATA4RXN AD9
 SATA4RXP AD8
 SATA4TXN AD6
 SATA4TXP AD5

 SATA5RXN AD3 NC SATA RXN5
 SATA5RXP AD1 NC SATA RXP5
 SATA5TXN AB7 NC SATA TXN5
 SATA5TXP AB1 NC SATA TXP5

 SATA1COMPO AF16
 SATA1COMPI AF15 R197 1

 P+ SATALED# T3

 SATA0GP / GPIO21 Y9 NC GPIO21 2
 SATA1GP / GPIO19 V1 NC GPIO19 2



Flash Descriptor Security	
High	Flash Descriptor will be in effect (default)
Low	Descriptor Security will be overridden

Title			
PCH(LPC,RTC,HDA,SATA)1/9			
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IBEX PEAK-M (PCI-E,SMBUS,CLK)

PCI-E* x1	Usage
Lane 1	UWB
Lane2	WWAN ->DEL
Lane 3	EXPRESS CARD -AUDIO BOARD
Lane 4	WLAN
Lane 5	NC
Lane 6	PHY
Lane 7	NC
Lane 8	NC

(35) PCIE_UWB_RX_N1
(35) PCIE_UWB_RX_P1
(35) PCIE_UWB_C_TX_N1
(35) PCIE_UWB_C_TX_P1

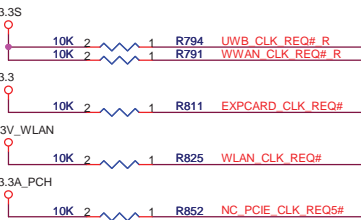
(45) PCIE_EXP_CARD_RX_N3
(45) PCIE_EXP_CARD_RX_P3
(45) PCIE_EXP_CARD_C_TX_N3
(45) PCIE_EXP_CARD_C_TX_P3

(34) PCIE_WLAN_RX_N4
(34) PCIE_WLAN_RX_P4
(34) PCIE_WLAN_C_TX_N4
(34) PCIE_WLAN_C_TX_P4

(47) PCIE_LAN_RX_N6
(47) PCIE_LAN_RX_P6
(47) PCIE_LAN_TX_N6
(47) PCIE_LAN_TX_P6

not
implemented

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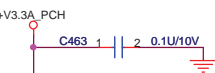
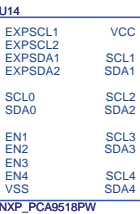
(35) CLK_PCIE_UWB#
(35) CLK_PCIE_UWB
(35) UWB_CLK_REQ#

(45) CLK_PCIE_EXP_CARD#
(45) CLK_PCIE_EXP_CARD
(45) EXP_CARD_CLK_REQ#

(34) CLK_PCIE_WLAN#
(34) CLK_PCIE_WLAN
(34) WLAN_CLK_REQ#

(47) CLK_PCIE_LAN#
(47) CLK_PCIE_LAN
(47) LAN_CLK_REQ#

SMBUS HUB



TO WLAN,UWB,ExpressCard

TO CLK_GEN,DDR3*2

TO G-Sensor

U9B

PERN1
PERP1
PETN1
PETP1

PERN2
PERP2
PETN2
PETP2

PERN3
PERP3
PETN3
PETP3

PERN4
PERP4
PETN4
PETP4

PERN5
PERP5
PETN5
PETP5

PERN6
PERP6
PETN6
PETP6

PERN7
PERP7
PETN7
PETP7

PERN8
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PETP8

PERN9
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PETP9

PERN10
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PERN11
PERP11
PETN11
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PERN20
PERP20
PETN20
PETP20

PERN21
PERP21
PETN21
PETP21

PERN22
PERP22
PETN22
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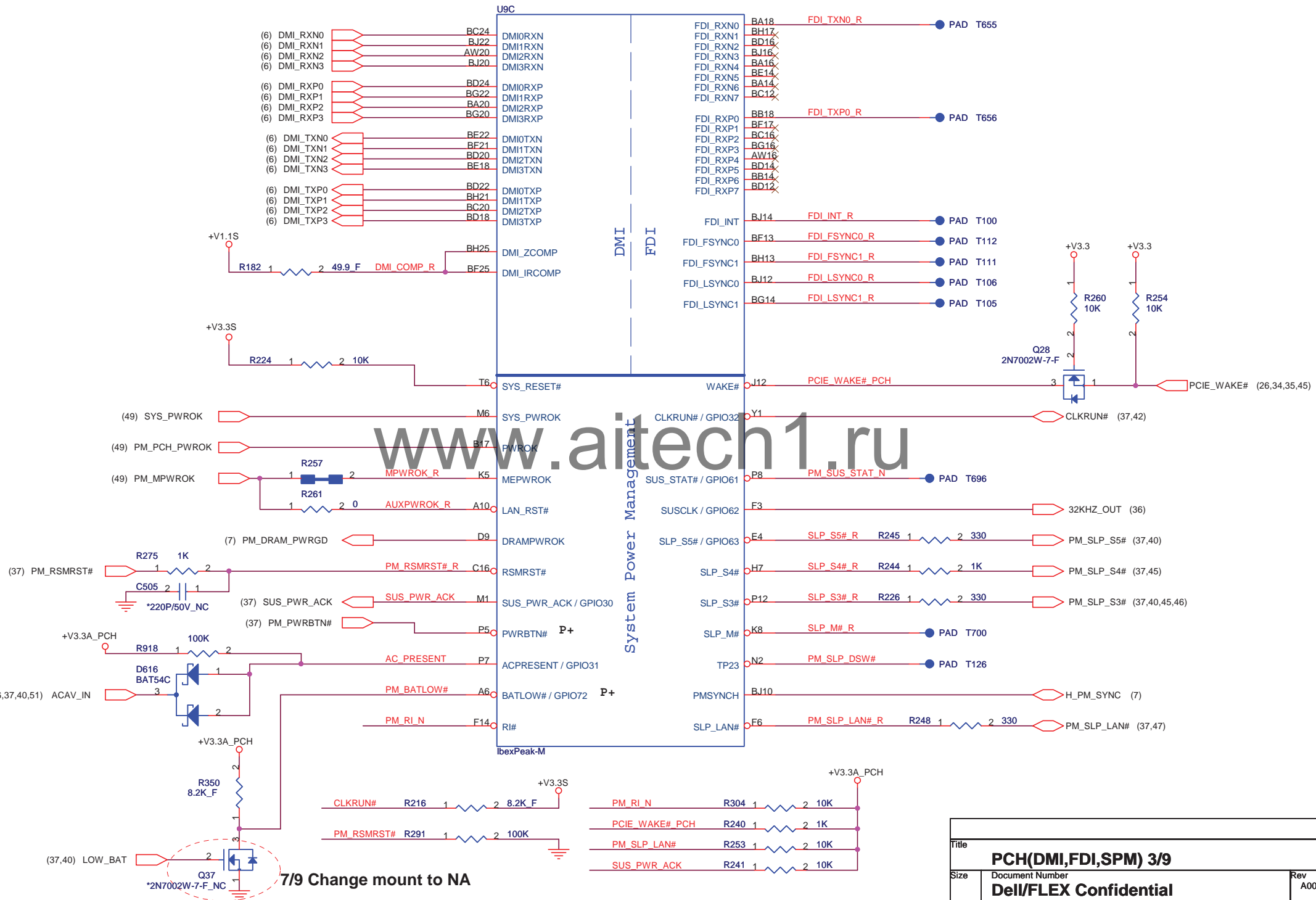
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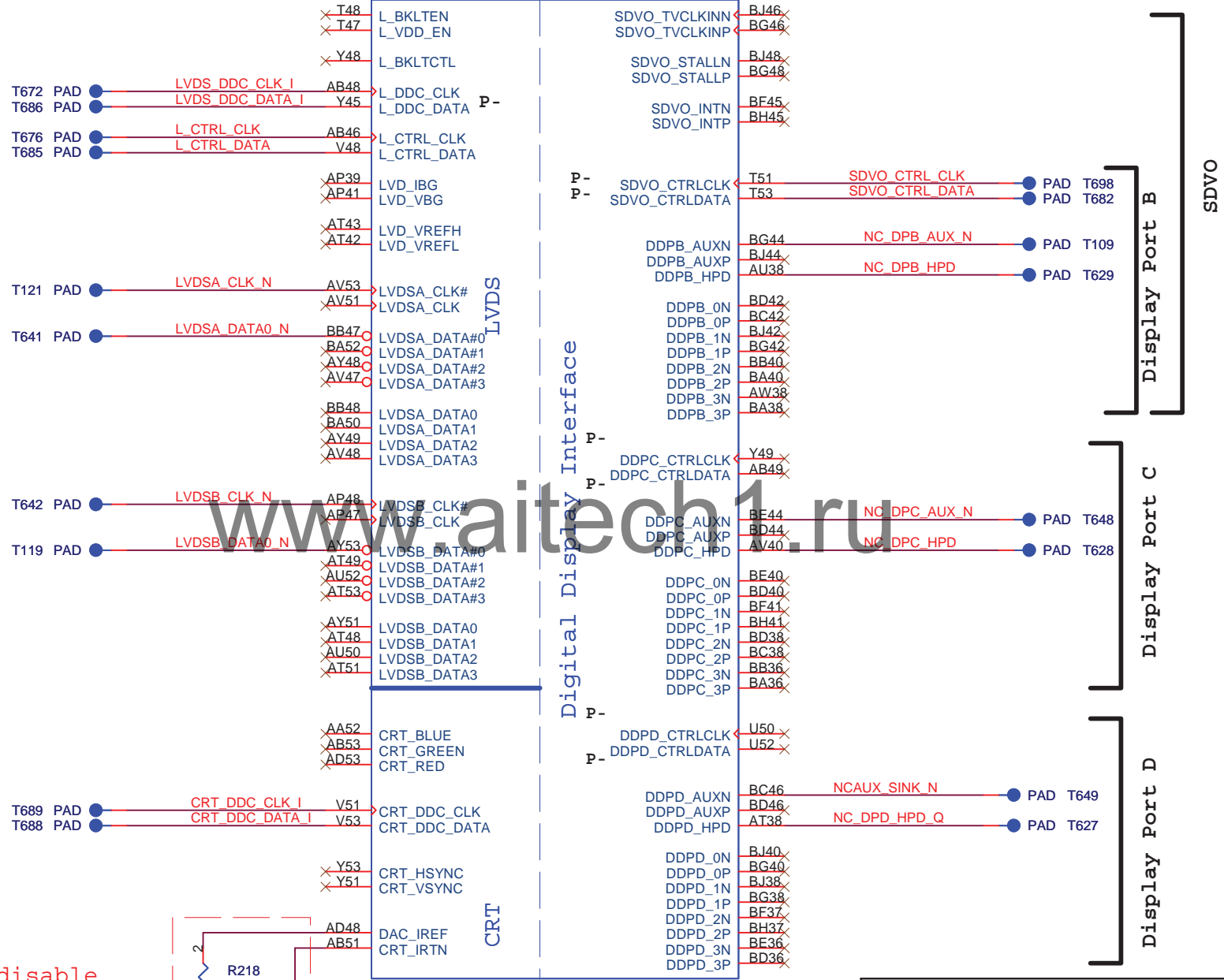
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IBEX PEAK-M (DMI,FDI,GPIO)



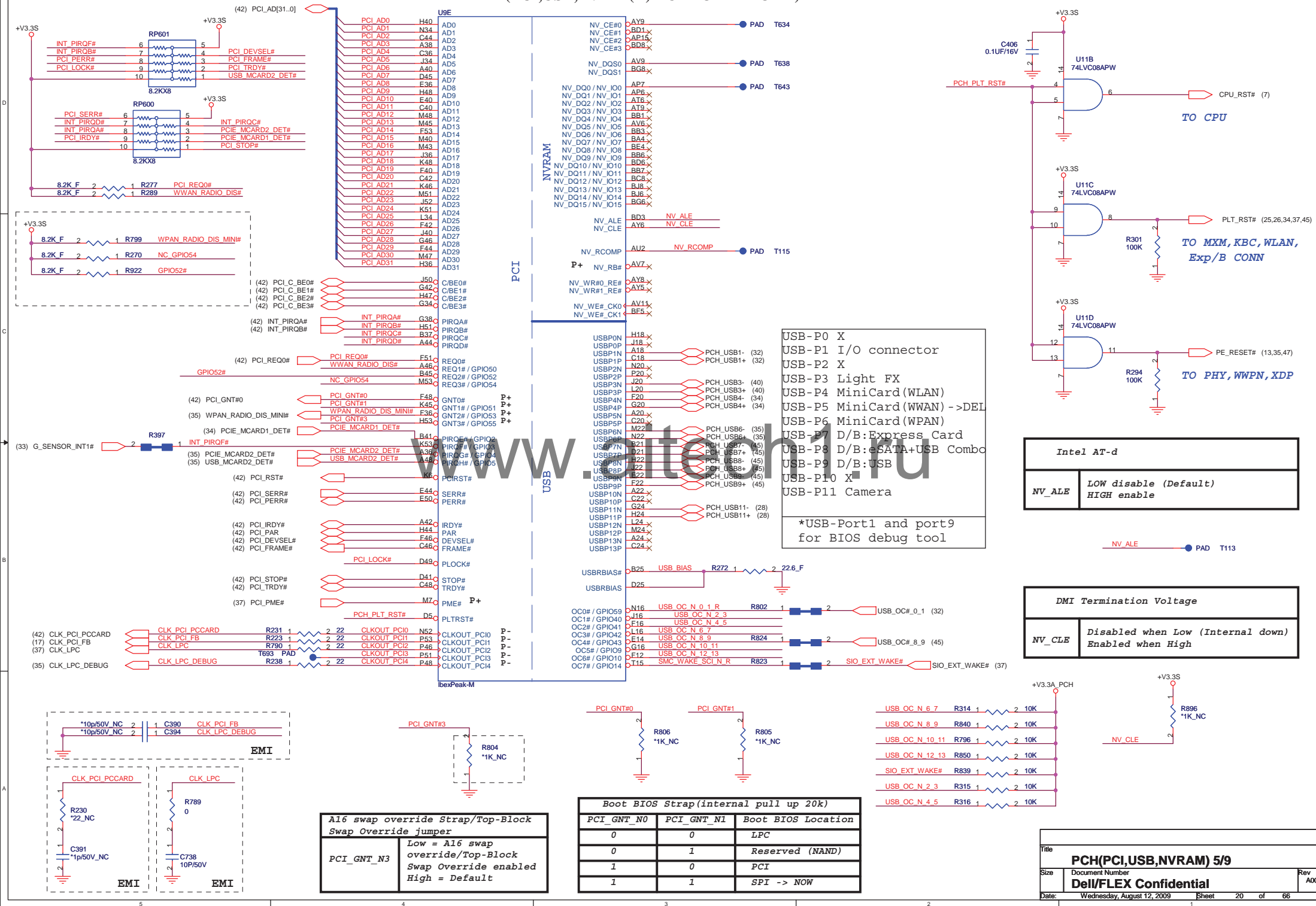
IBEX PEAK-M (LVDS,DDI)

U9D



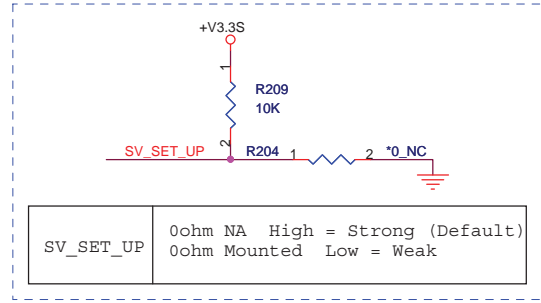
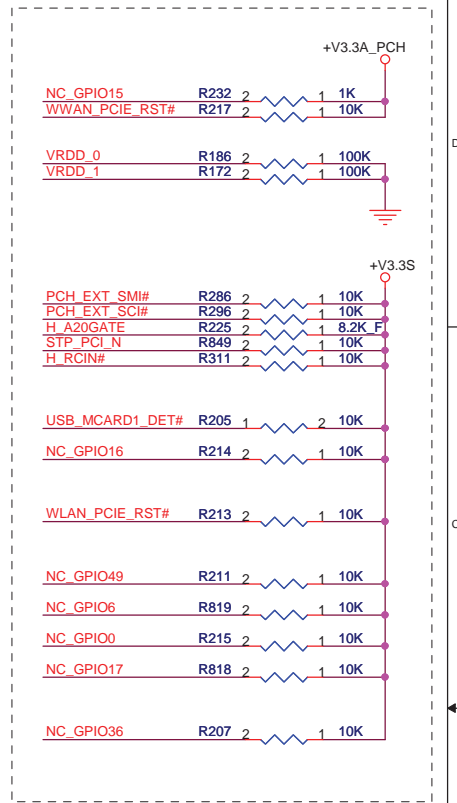
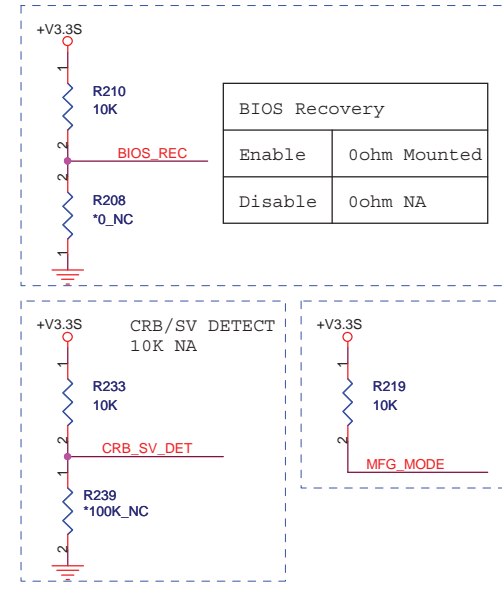
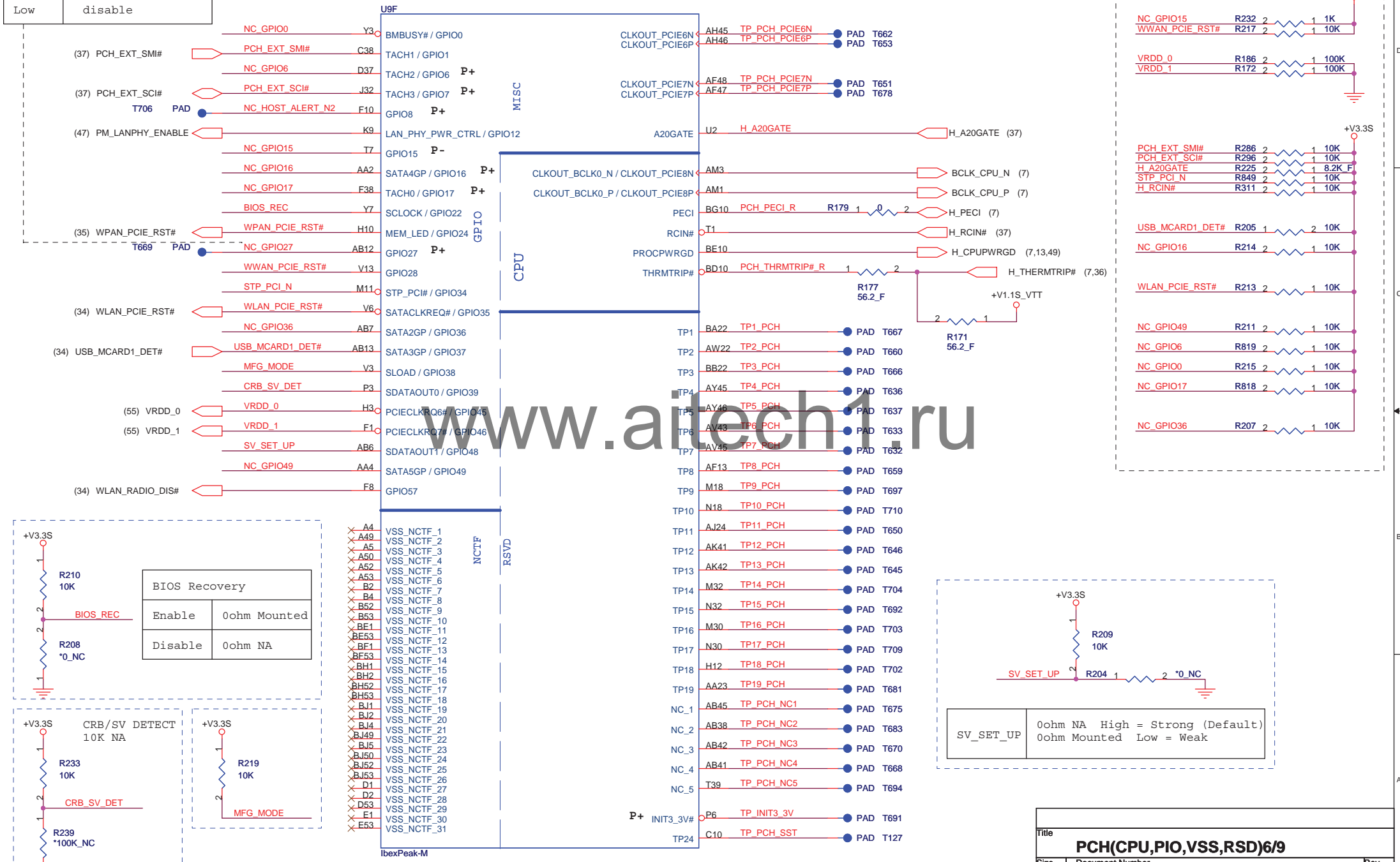
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PCH(CRT,LVDS,DDI) 4/9		
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IBEX PEAK-M (PCI,USB,INTEL(R) TURBO MEMORY)

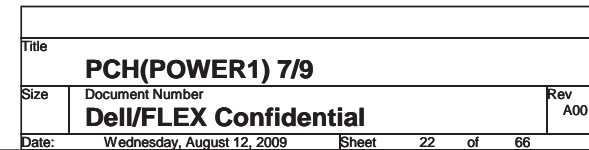


On-Die PLL voltage regulator	
High	enable(default)
Low	disable

IBEX PEAK-M(GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M(POWER)



IBEX PEAK-M(POWER)

POWER

USB

Clock and Miscellaneous

PCI/GPIO/LPC

SATA

PCI/GPIO/LPC

CPU

RTC

HDA

VCCIO Total
3062mA

VCCSUS3_3 Total
163mA

VCC3_3 Total
357mA

31mA

6mA

VCCME Total
3062mA

320mA

52mA

2mA

Please note that all Ibex Peak-M rails with netnames +V1.1S and +V1.1M rails are actually +V1.05S and +V1.05M rails

Close to PCH

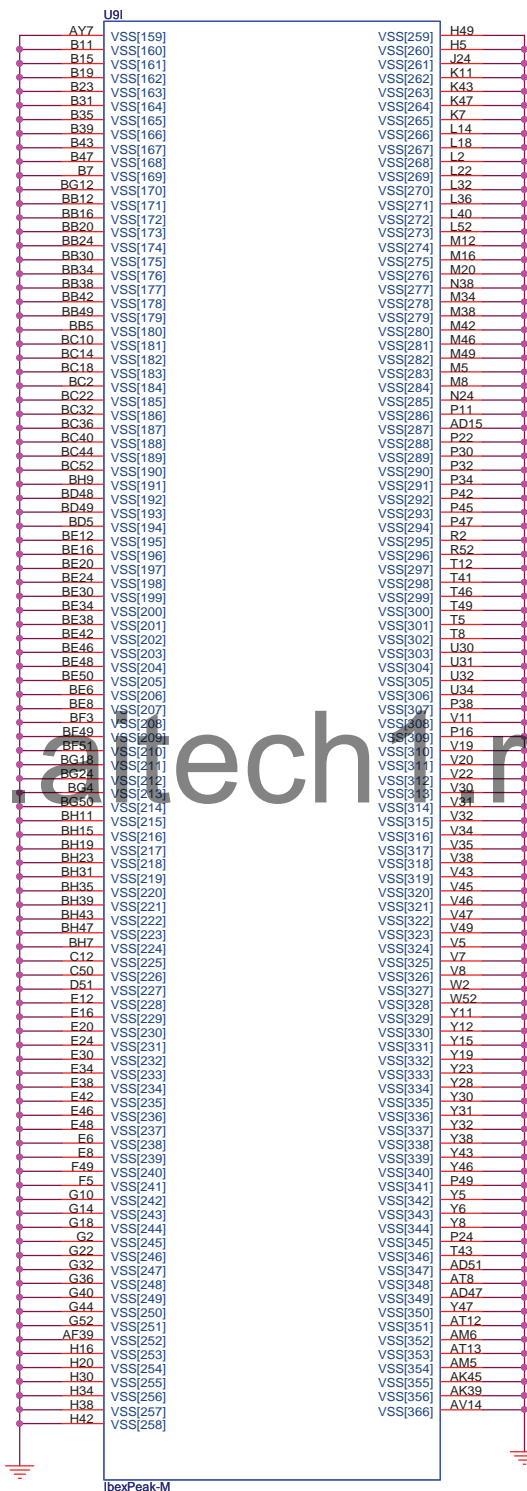
+V5A1 has off during S4/S5 battery mode.

<1mA

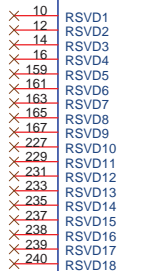
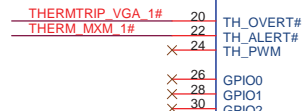
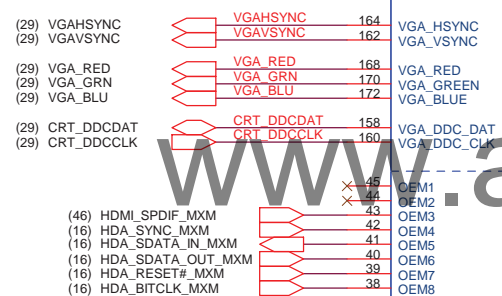
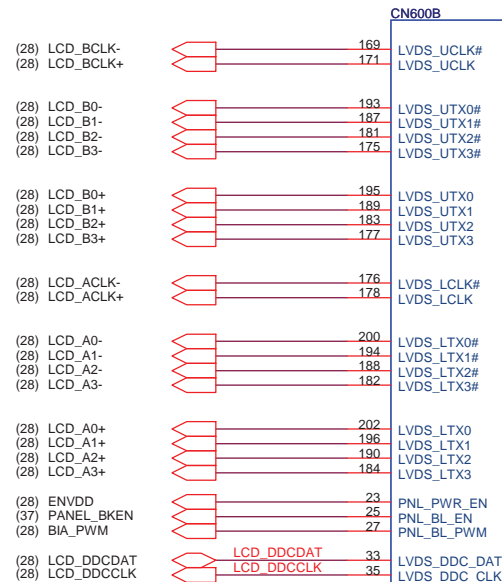
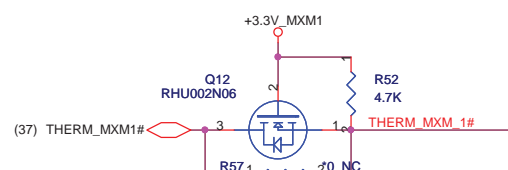
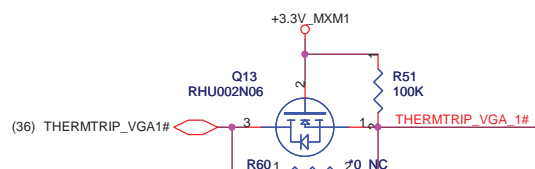
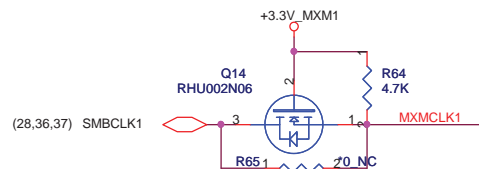
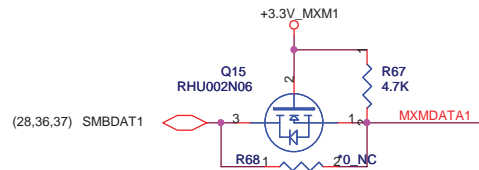
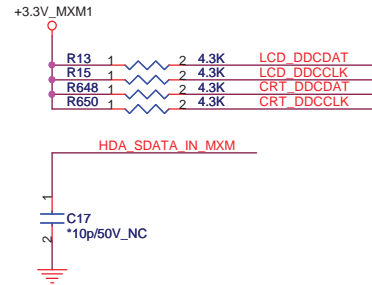
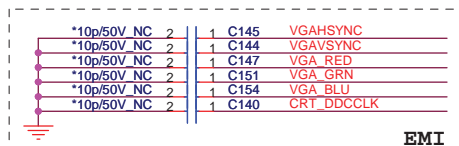
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			Rev A00		

U9H		
AB16	VSS[0]	
AA19	VSS[1]	VSS[80]
AA20	VSS[2]	VSS[81]
AA22	VSS[3]	VSS[82]
AM19	VSS[4]	VSS[83]
AA24	VSS[5]	VSS[84]
AA26	VSS[6]	VSS[85]
AA28	VSS[7]	VSS[86]
AA30	VSS[8]	VSS[87]
AA31	VSS[9]	VSS[88]
AA32	VSS[10]	VSS[89]
AB11	VSS[11]	VSS[90]
AB15	VSS[12]	VSS[91]
AB23	VSS[13]	VSS[92]
AB30	VSS[14]	VSS[93]
AB31	VSS[15]	VSS[94]
AB32	VSS[16]	VSS[95]
AB39	VSS[17]	VSS[96]
AB43	VSS[18]	VSS[97]
AB47	VSS[19]	VSS[98]
AB5	VSS[20]	VSS[99]
AB8	VSS[21]	VSS[100]
AC2	VSS[22]	VSS[101]
AC52	VSS[23]	VSS[102]
AD11	VSS[24]	VSS[103]
AD12	VSS[25]	VSS[104]
AD16	VSS[26]	VSS[105]
AD23	VSS[27]	VSS[106]
AD30	VSS[28]	VSS[107]
AD31	VSS[29]	VSS[108]
AD32	VSS[30]	VSS[109]
AD34	VSS[31]	VSS[110]
AU22	VSS[32]	VSS[111]
AD42	VSS[33]	VSS[112]
AD46	VSS[34]	VSS[113]
AD49	VSS[35]	VSS[114]
AD7	VSS[36]	VSS[115]
AE2	VSS[37]	VSS[116]
AE4	VSS[38]	VSS[117]
AF12	VSS[39]	VSS[118]
Y13	VSS[40]	VSS[119]
AH49	VSS[41]	VSS[120]
AU4	VSS[42]	VSS[121]
AF35	VSS[43]	VSS[122]
AP13	VSS[44]	VSS[123]
AN34	VSS[45]	VSS[124]
AF45	VSS[46]	VSS[125]
AF46	VSS[47]	VSS[126]
AF49	VSS[48]	VSS[127]
AF5	VSS[49]	VSS[128]
AF8	VSS[50]	VSS[129]
AG2	VSS[51]	VSS[130]
AG52	VSS[52]	VSS[131]
AH11	VSS[53]	VSS[132]
AH15	VSS[54]	VSS[133]
AH16	VSS[55]	VSS[134]
AH24	VSS[56]	VSS[135]
AH32	VSS[57]	VSS[136]
AH43	VSS[58]	VSS[137]
AH47	VSS[59]	VSS[138]
AH7	VSS[60]	VSS[139]
AH19	VSS[61]	VSS[140]
AJ2	VSS[62]	VSS[141]
AJ20	VSS[63]	VSS[142]
AJ22	VSS[64]	VSS[143]
AJ23	VSS[65]	VSS[144]
AJ26	VSS[66]	VSS[145]
AJ28	VSS[67]	VSS[146]
AJ32	VSS[68]	VSS[147]
AJ34	VSS[69]	VSS[148]
AT5	VSS[70]	VSS[149]
AJ4	VSS[71]	VSS[150]
AK12	VSS[72]	VSS[151]
AM1	VSS[73]	VSS[152]
AM19	VSS[74]	VSS[153]
AK26	VSS[75]	VSS[154]
AK22	VSS[76]	VSS[155]
AK23	VSS[77]	VSS[156]
AK28	VSS[78]	VSS[157]
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		AM11
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		AP5



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JAE_MM70-314-310B1-2

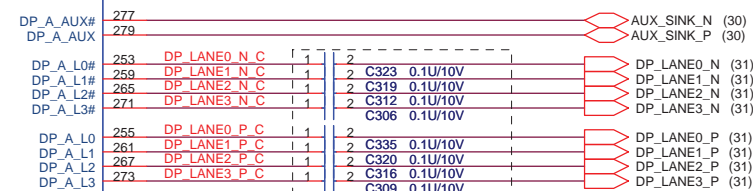
MXM Conn

DP-A

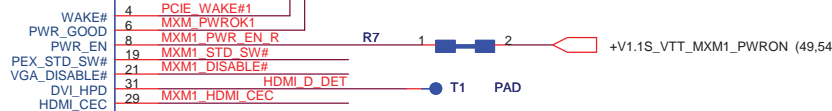
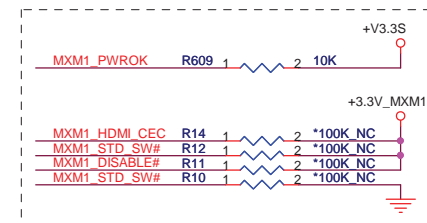
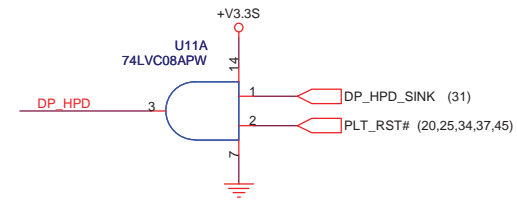
DP-B

DP-C

DP-D



Close DP CONN CN10



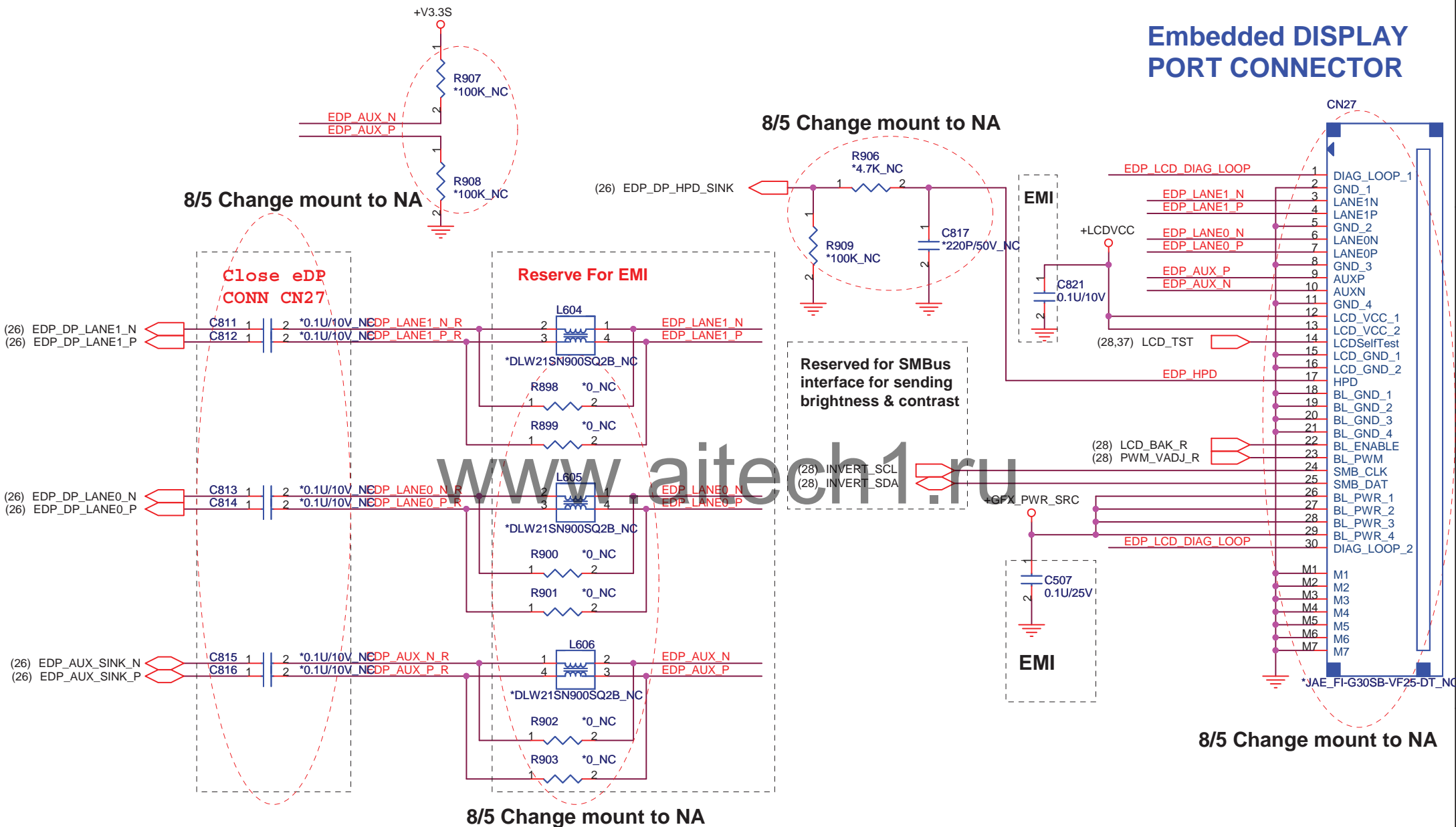
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Embedded DISPLAY PORT CONNECTOR

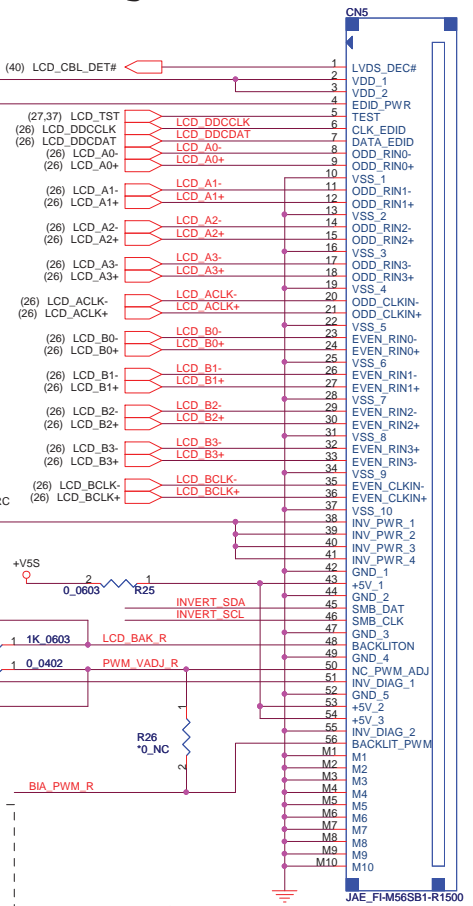
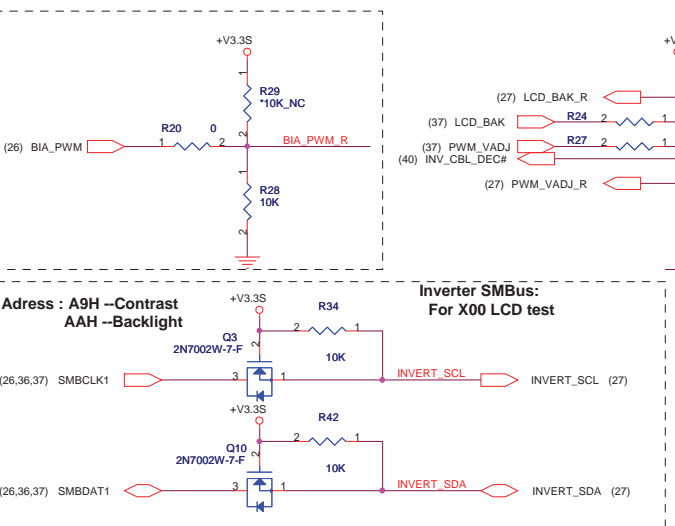
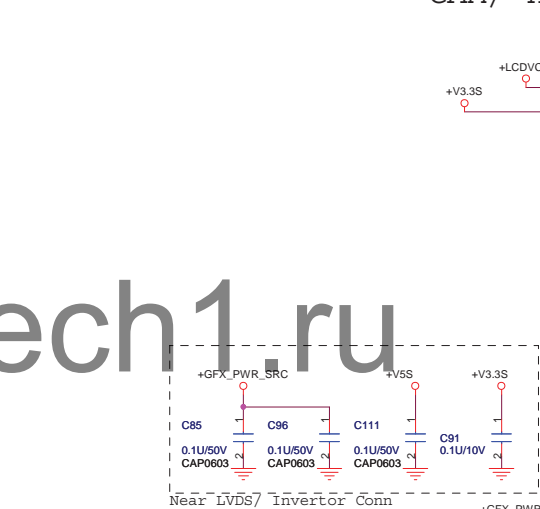
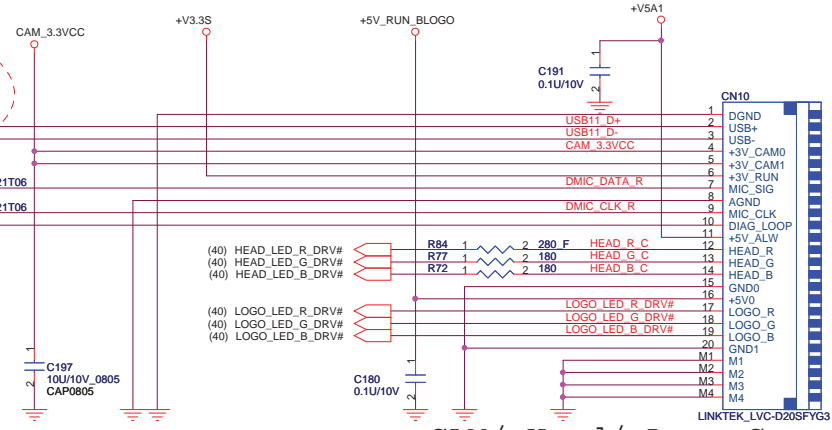
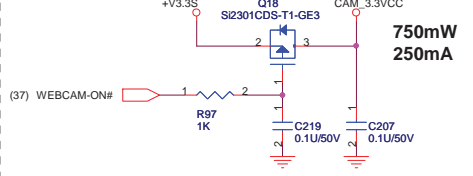
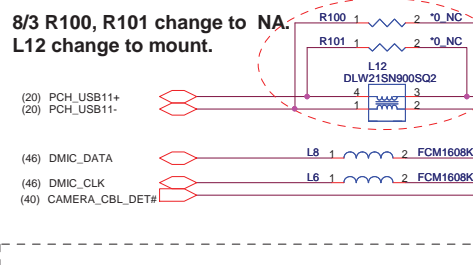
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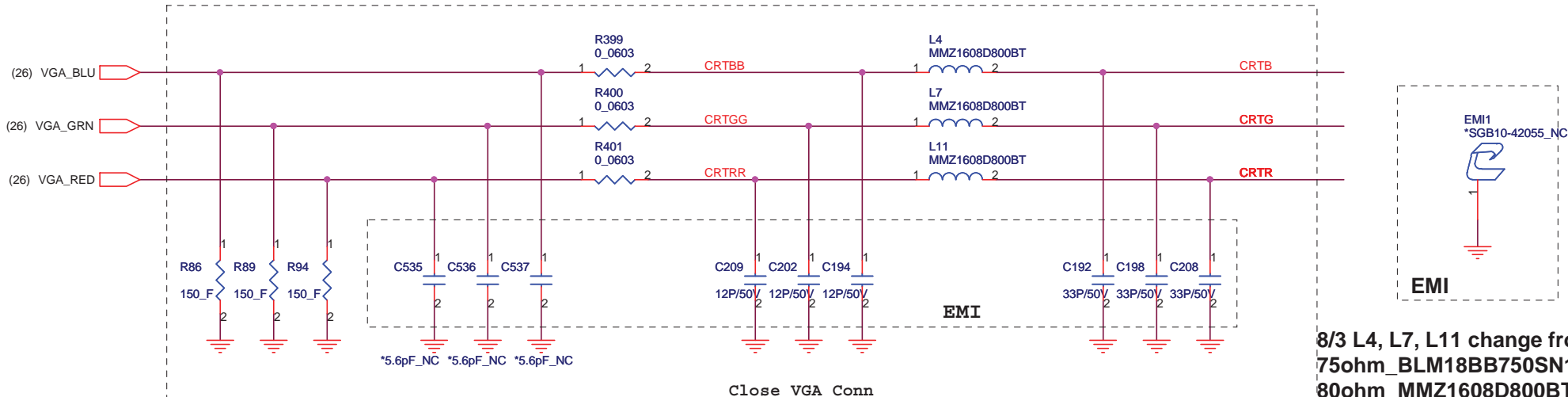


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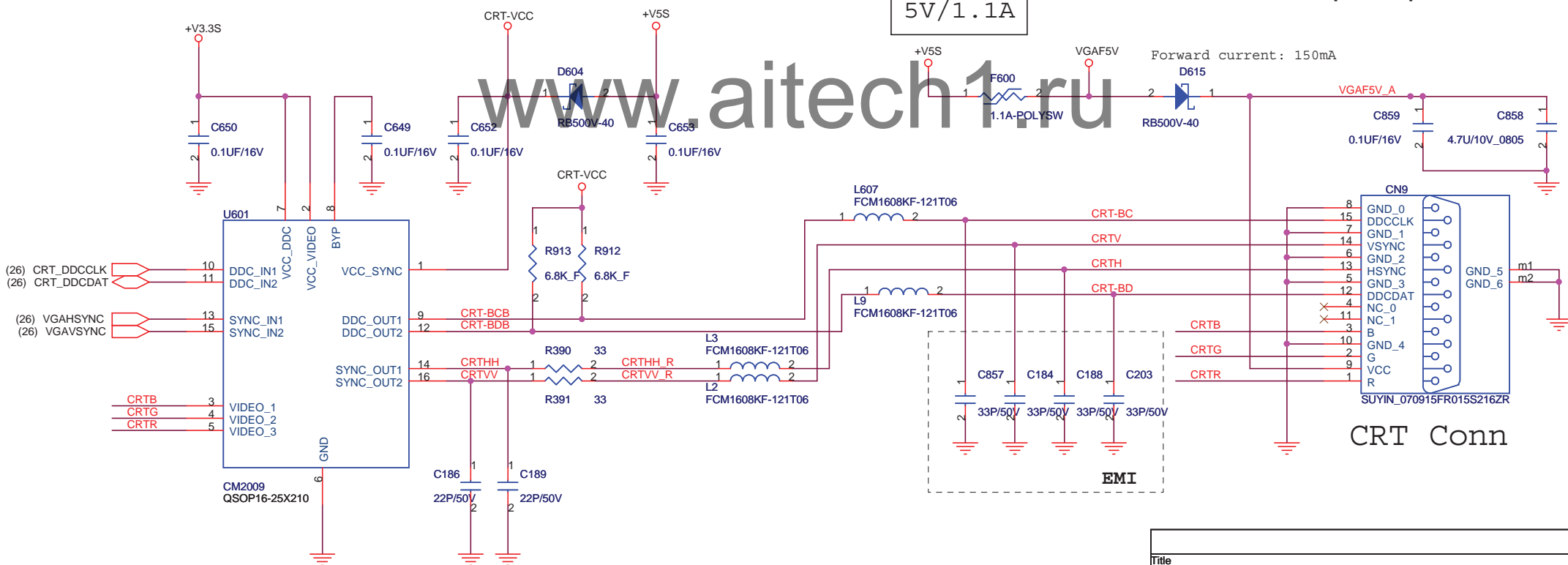


LVDS/ Invertor Conn

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LCD CONN				
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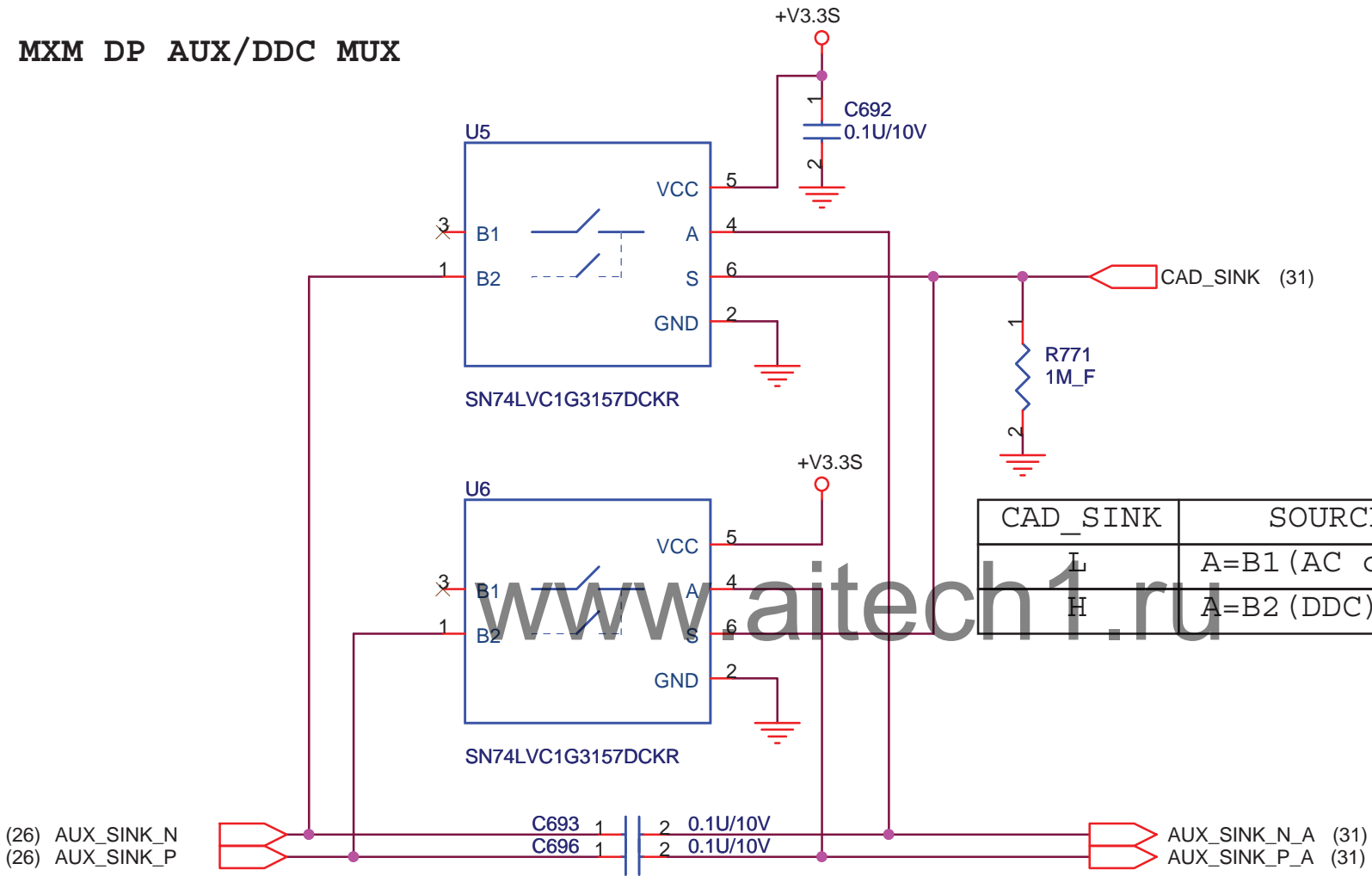


8/3 L4, L7, L11 change from 75ohm_BLM18BB750SN1D to 80ohm_MMZ1608D800BT. C209, C202, C194 change from 18pF to 12pF. C192, C198, C208 change from 18pF to 33pF.



Title		
CRT CONN		
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MXM DP AUX/DDC MUX



CAD_SINK	SOURCE	Function
L	A=B1 (AC couple)	DP Path
H	A=B2 (DDC)	HDMI Path

(26) DP_LANE3_N
(26) DP_LANE3_P

DP_LANE3_N
DP_LANE3_P

L21

*DLW21SN900SQ2B_NC

R157 0
R159 0

DP_LANE3_N R
DP_LANE3_P R

(26) DP_LANE2_N
(26) DP_LANE2_P

DP_LANE2_N
DP_LANE2_P

L22

*DLW21SN900SQ2B_NC

R160 0
R162 0

DP_LANE2_N R
DP_LANE2_P R

(26) DP_LANE1_N
(26) DP_LANE1_P

DP_LANE1_N
DP_LANE1_P

L23

*DLW21SN900SQ2B_NC

R164 0
R166 0

DP_LANE1_N R
DP_LANE1_P R

(26) DP_LANE0_N
(26) DP_LANE0_P

DP_LANE0_N
DP_LANE0_P

L24

*DLW21SN900SQ2B_NC

R167 0
R170 0

DP_LANE0_N R
DP_LANE0_P R

(30) AUX_SINK_N_A
(30) AUX_SINK_P_A

AUX_SINK_N_A
AUX_SINK_P_A

L20

*DLW21SN900SQ2B_NC

R153 0
R155 0

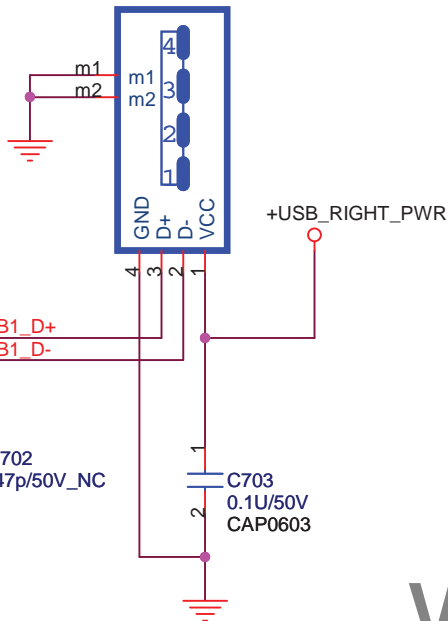
AUX_SINK_N R
AUX_SINK_P R

[illegible]

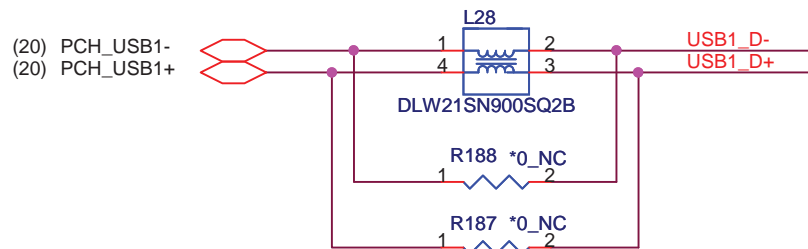
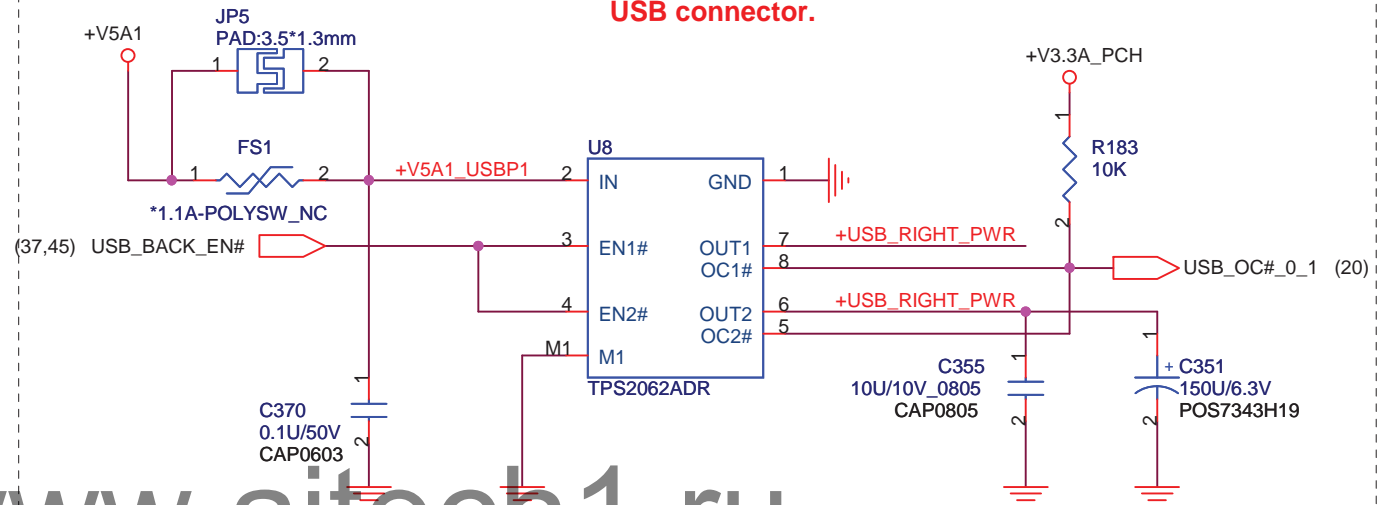
Title			
DP CONN			
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USB CONN

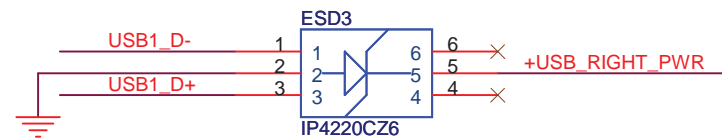
CN15
FOXCONN_UB9112C-CA201-9F



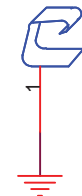
USB POWER SW



Place ESD diodes as close as USB connector.

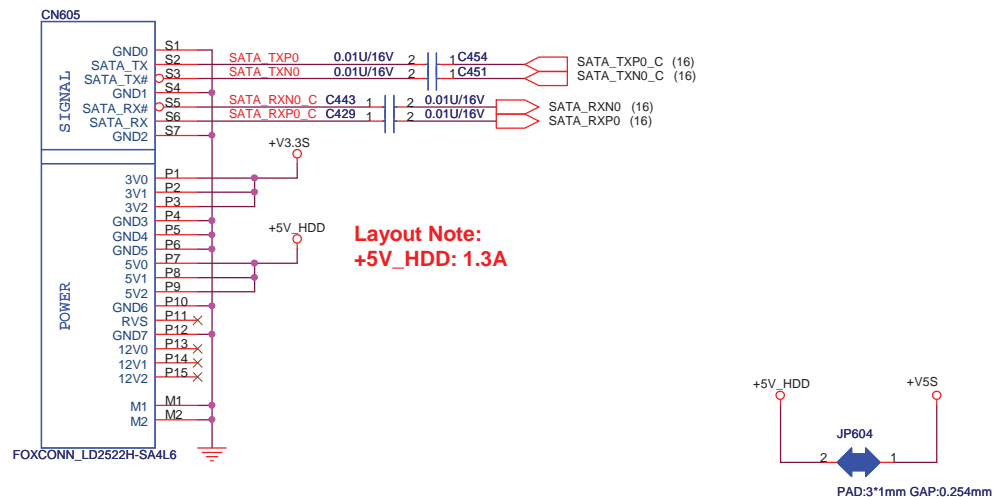


EMI604
*SGB10-42055_NC

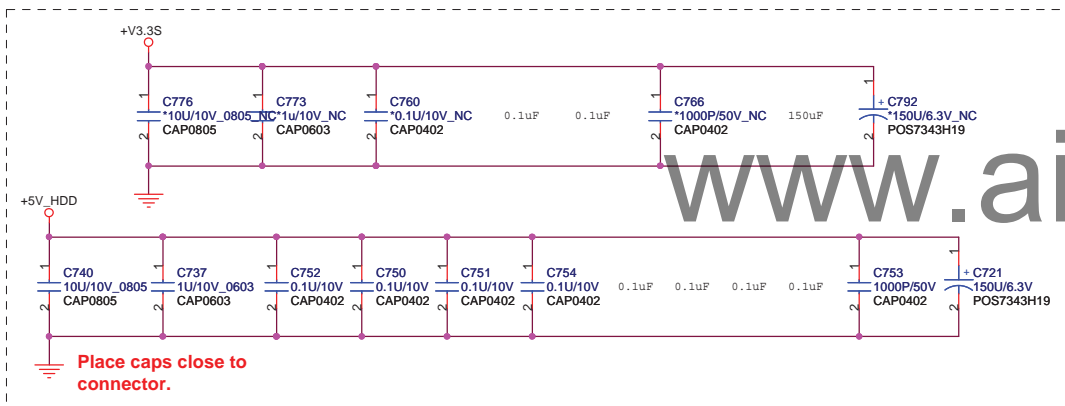


EMI

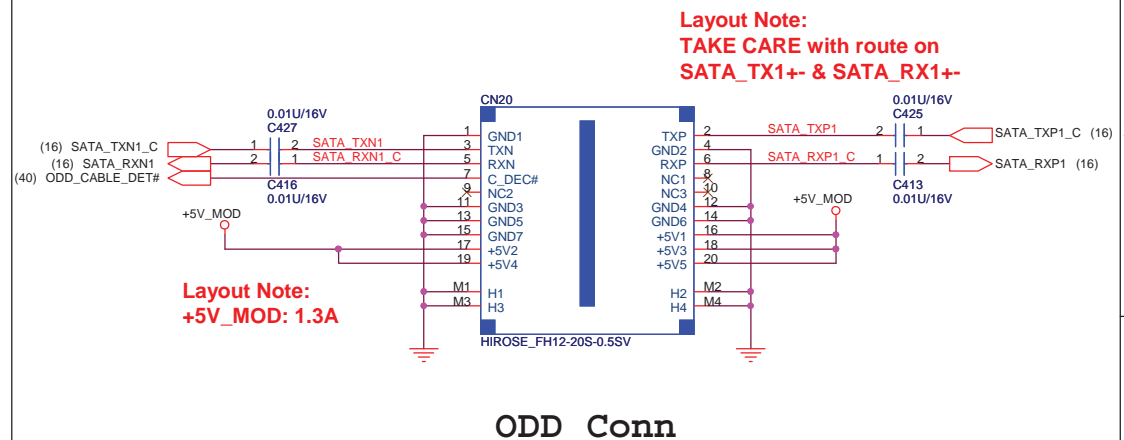
Title			
USB			
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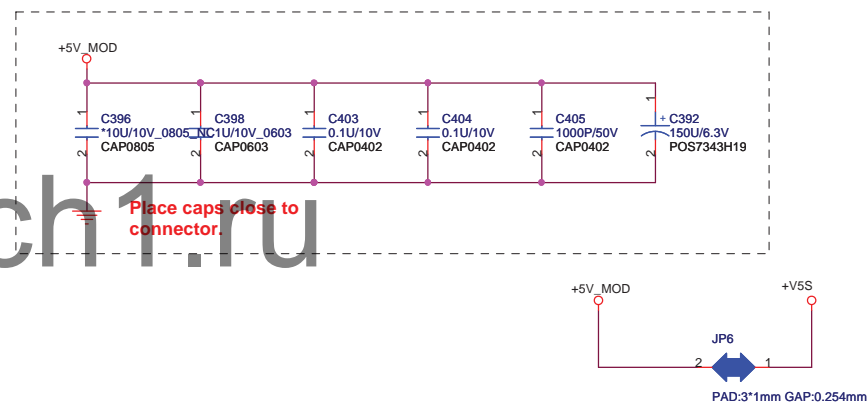
HDD Conn



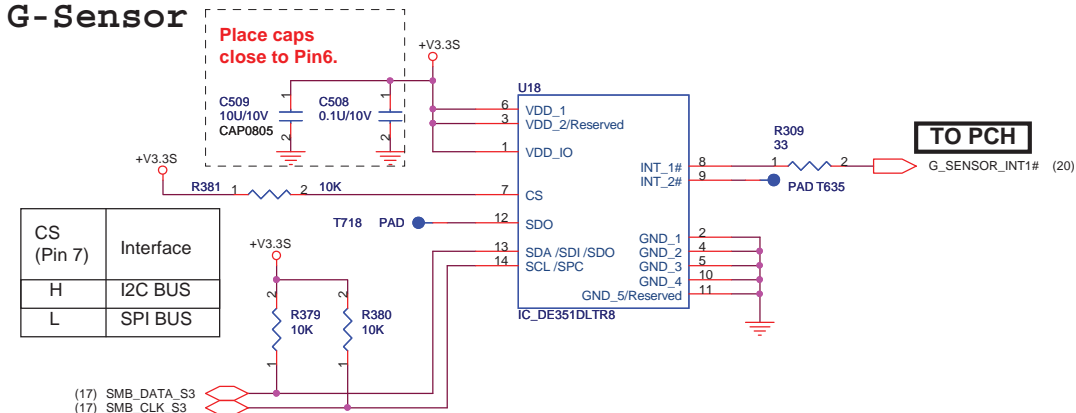
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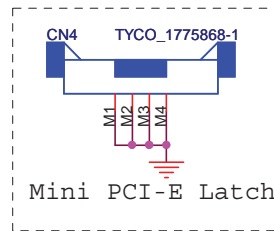


ODD Conn



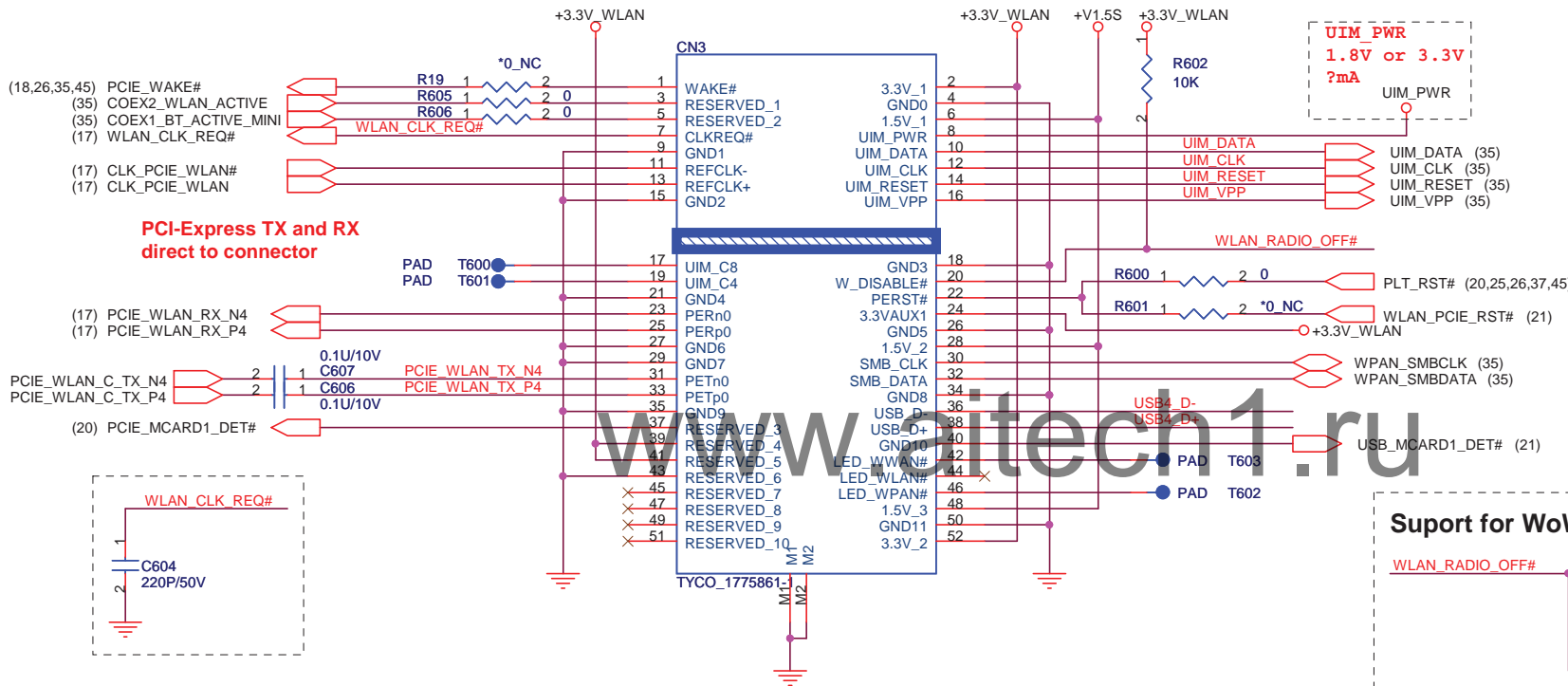
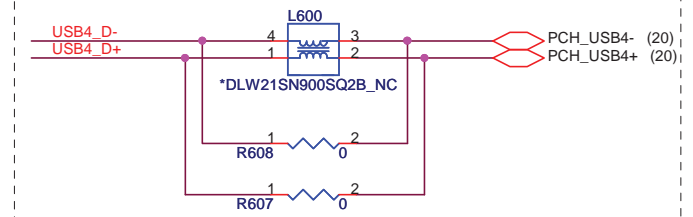
G-Sensor



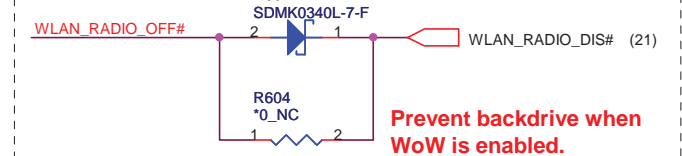


MiniCard WLAN Connector

Reserved PAD for EMI

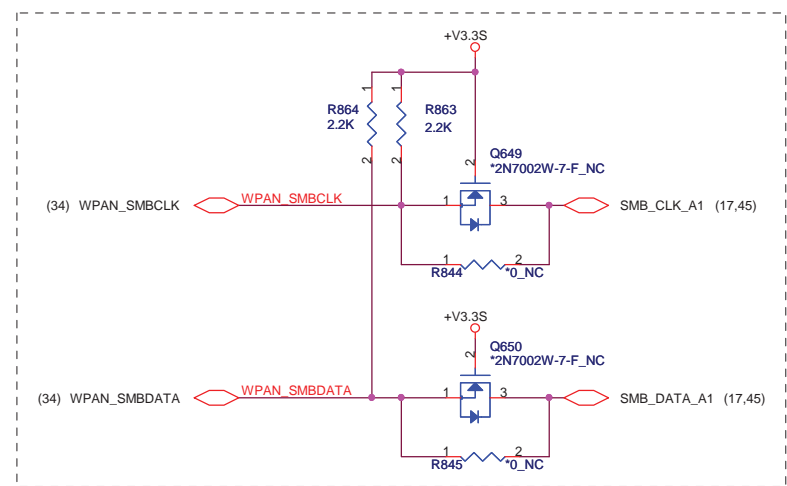
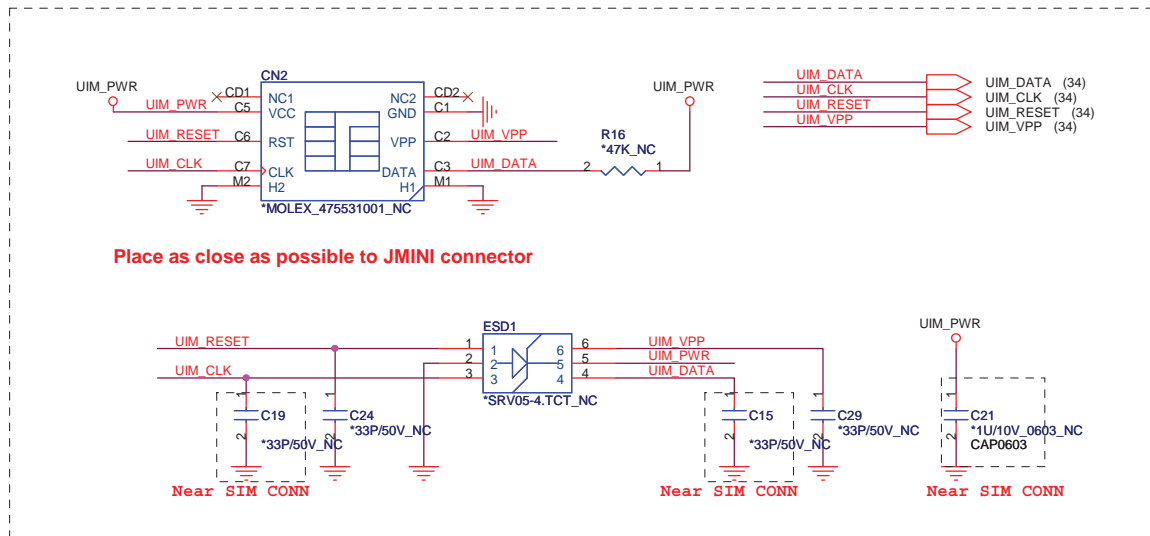
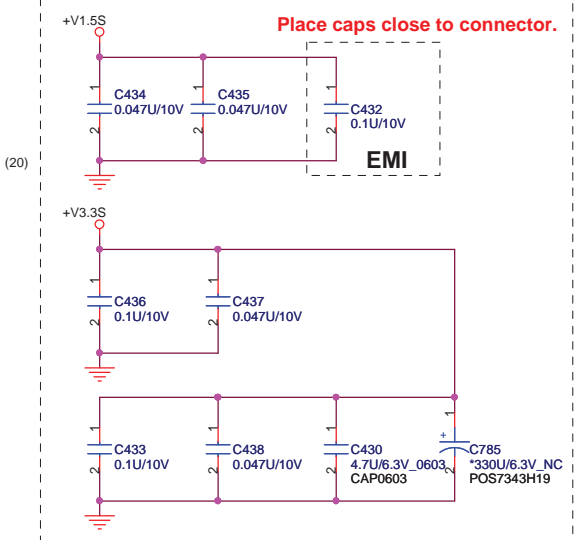
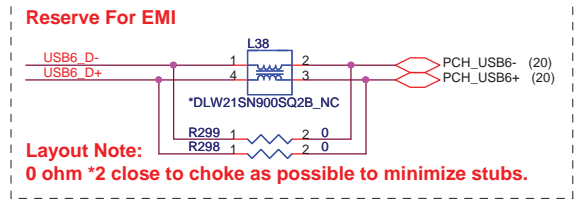
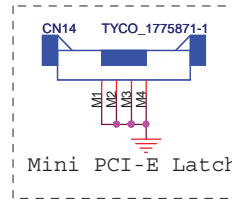
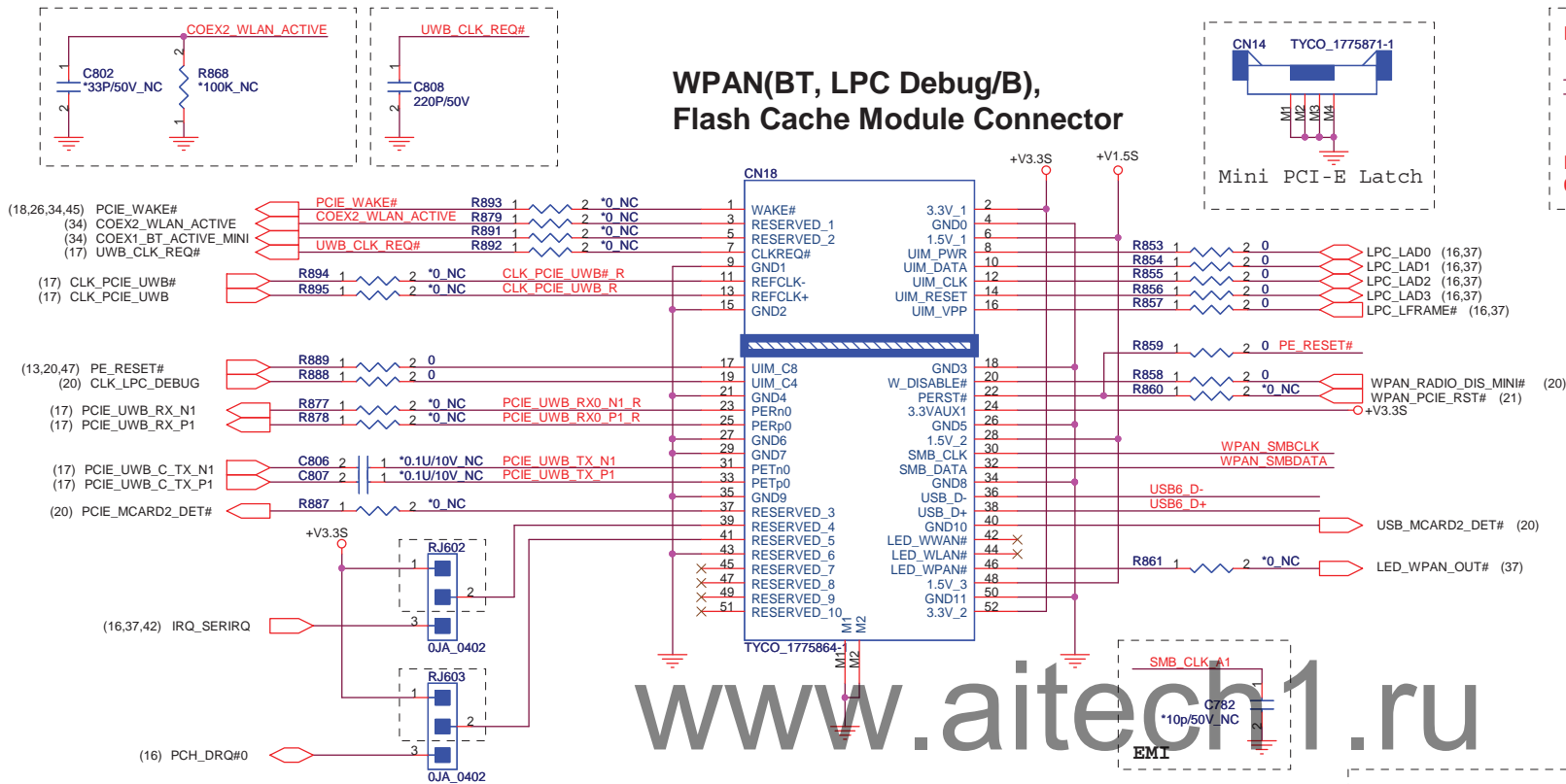


Support for WoW

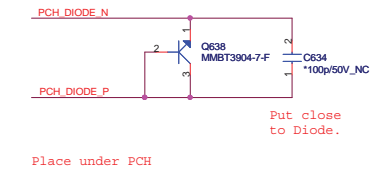
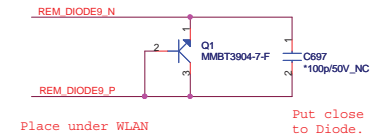
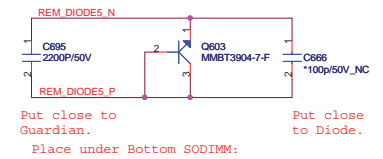
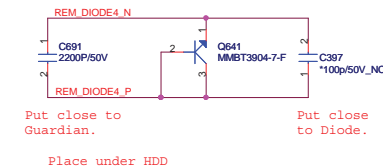
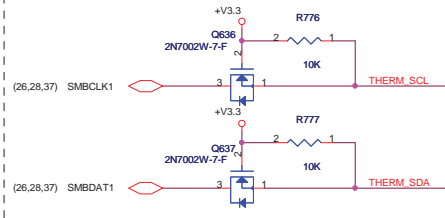
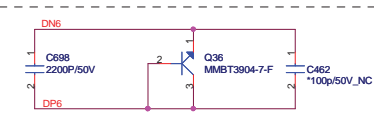
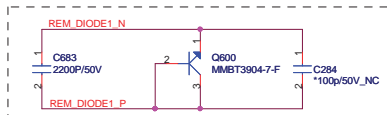


Title		
MINI-CARD (WLAN)		
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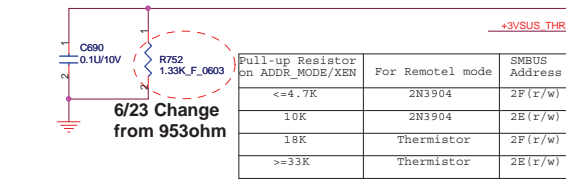
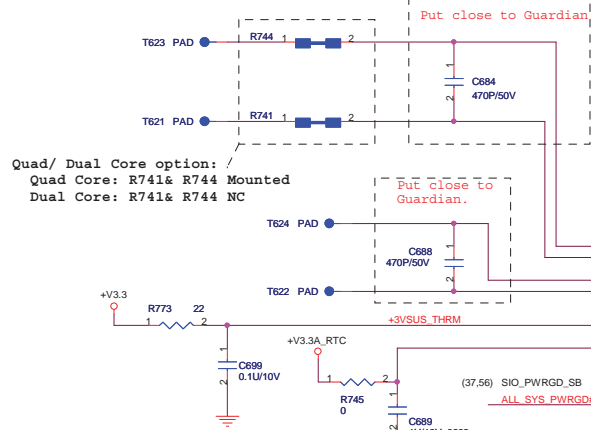
WPAN(BT, LPC Debug/B), Flash Cache Module Connector



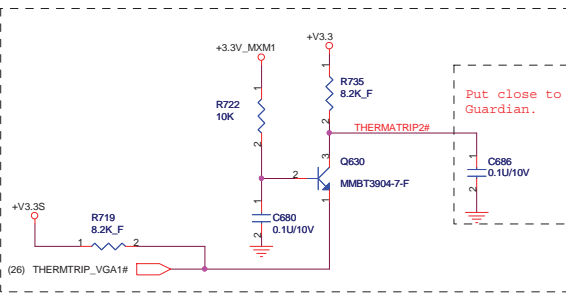
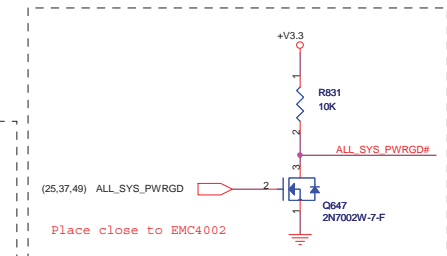
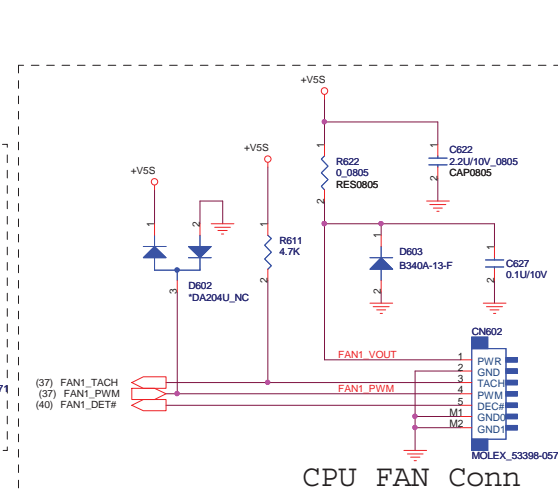
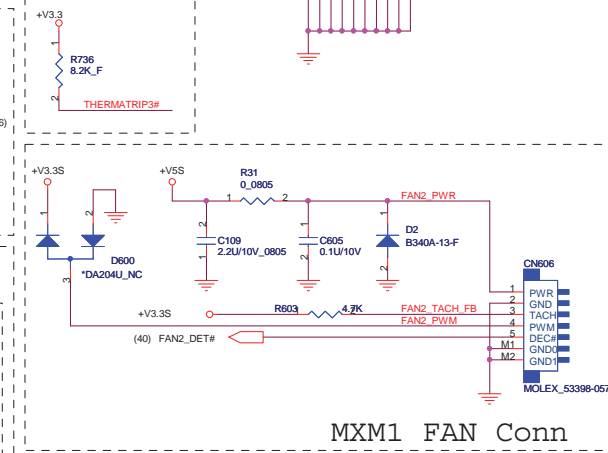
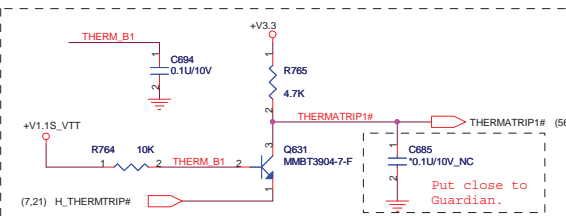
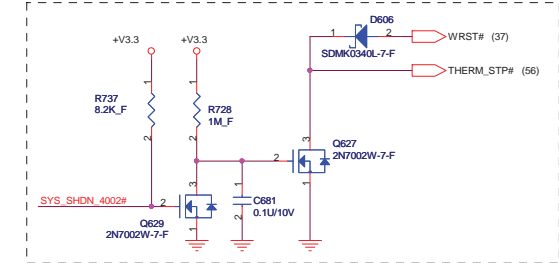
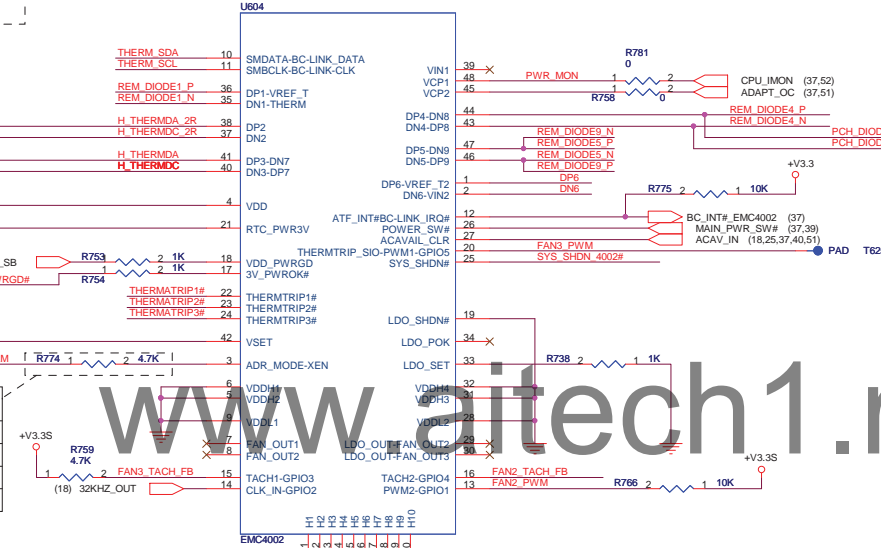
Title			
MINI-CARD (WPAN,WWAN)			
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Quad/ Dual Core option:
Quad Core: R741& R744 Mounted
Dual Core: R741& R744 NC

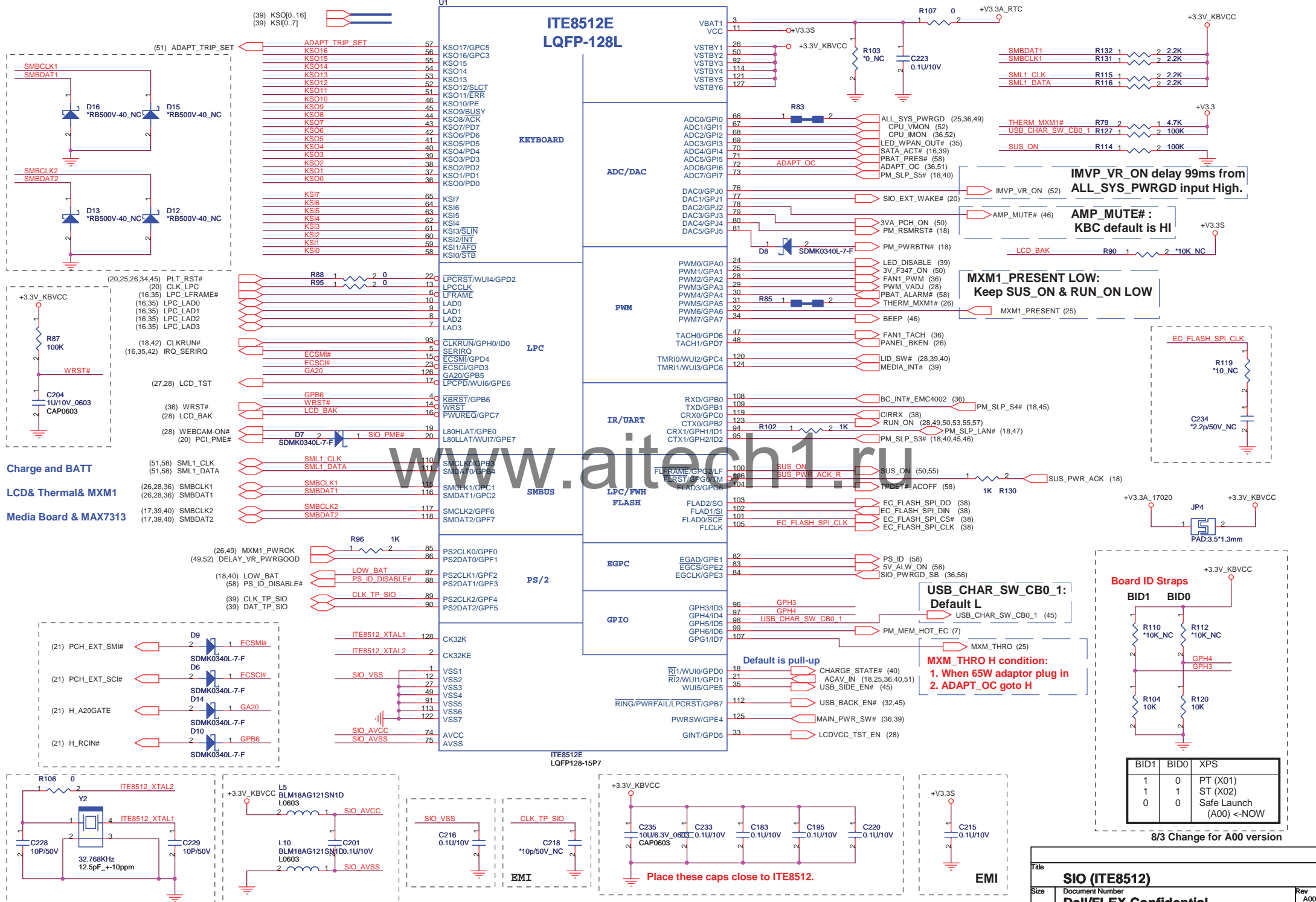


Full-up Resistor or ADDR_MODE/XEN	For Remotel mode	SMBUS Address
<=4.7K	2N3904	2F (r/w)
10K	2N3904	2E (r/w)
18K	Thermistor	2F (r/w)
>=33K	Thermistor	2E (r/w)

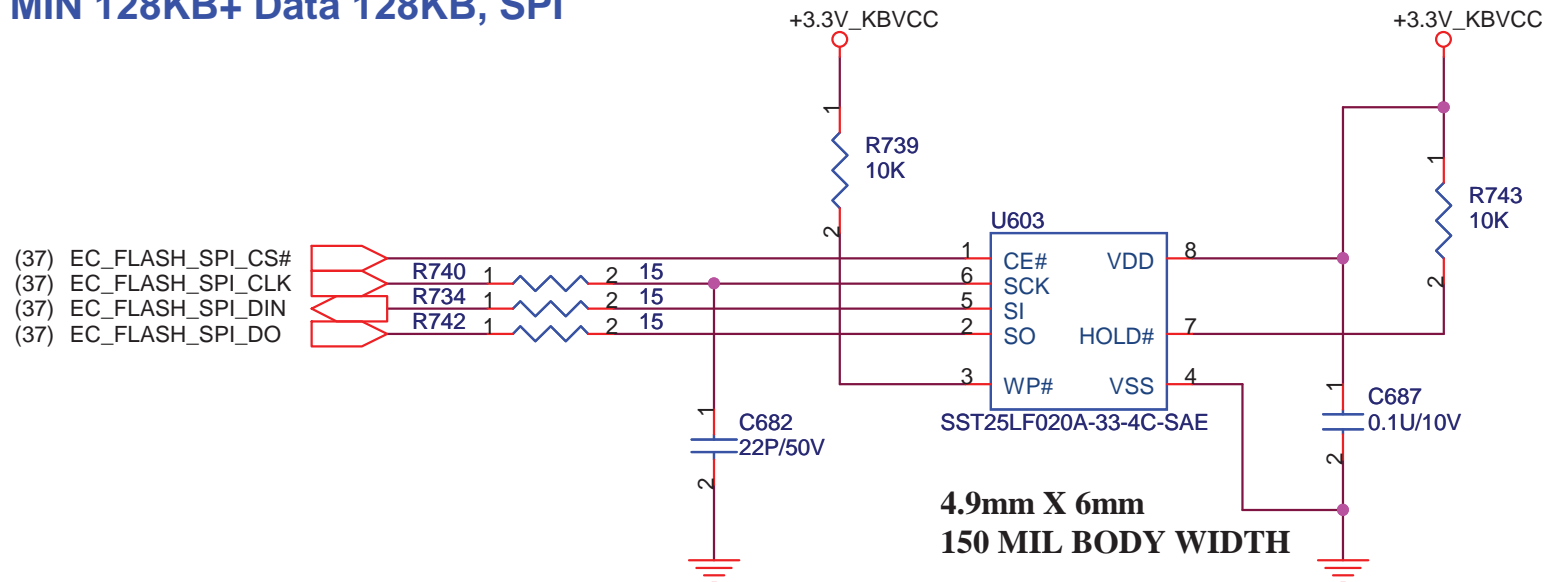


MXM1 FAN Conn

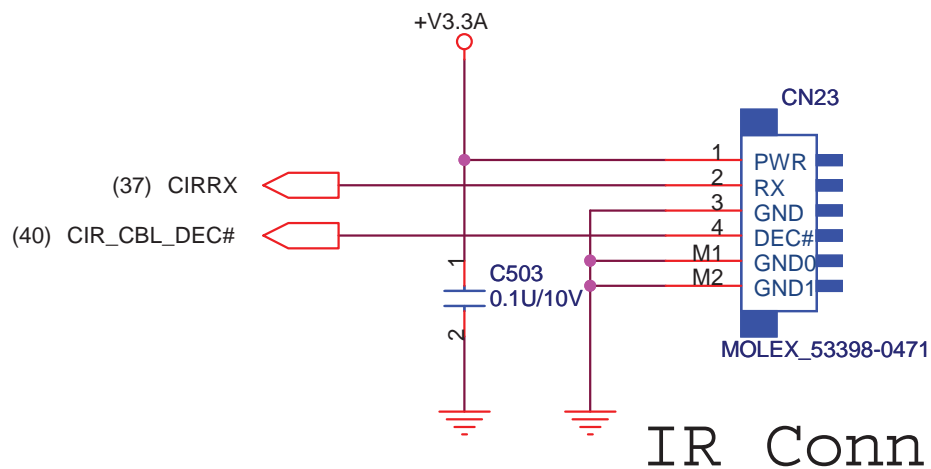
CPU FAN Conn



MIN 128KB+ Data 128KB, SPI



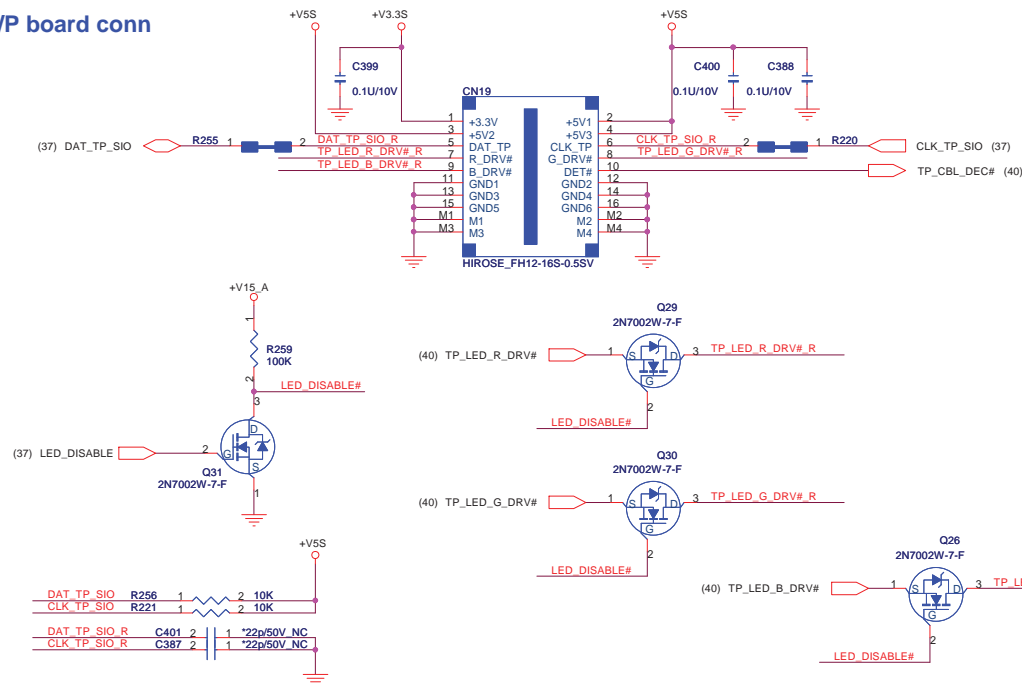
to Consumer IR



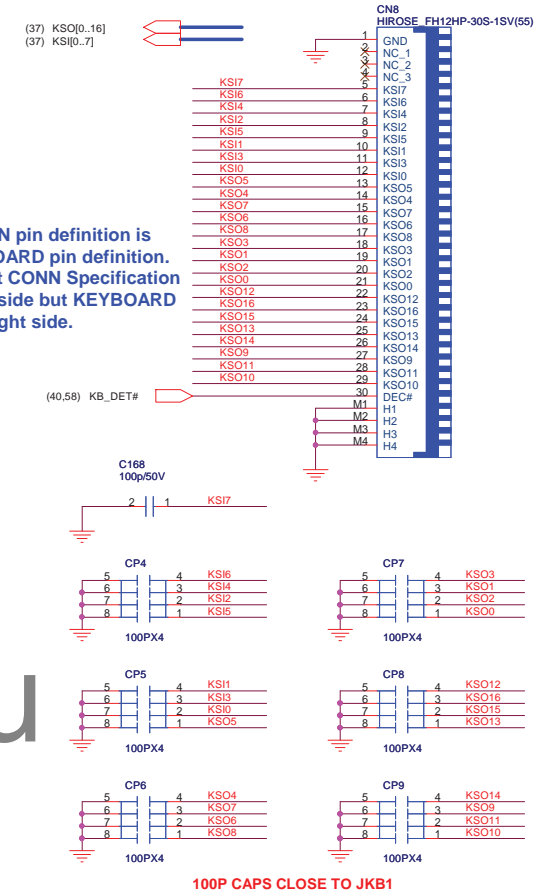
IR Conn

Title		
FLASH/ CIR		
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T/P board conn



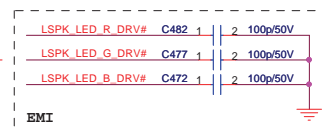
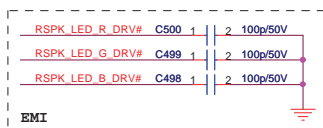
KEYBOARD CONNECTOR



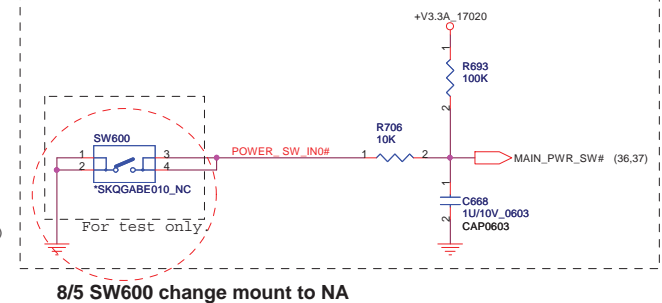
KEYBOARD CONN pin definition is reverse of KEYBOARD pin definition. This is cause that CONN Specification order pin1 in left side but KEYBOARD cable pin1 is in right side.

Right SPK LED Conn

Left SPK LED Conn

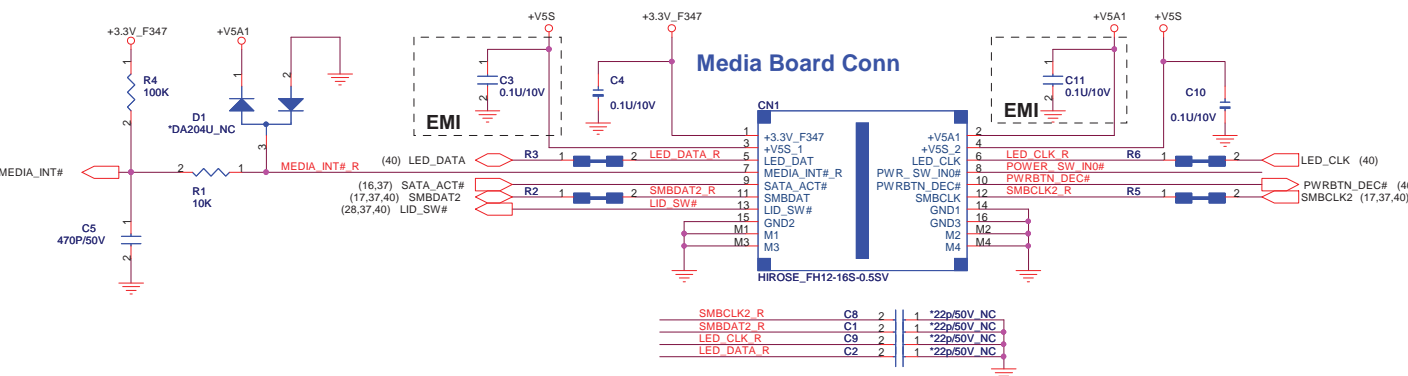


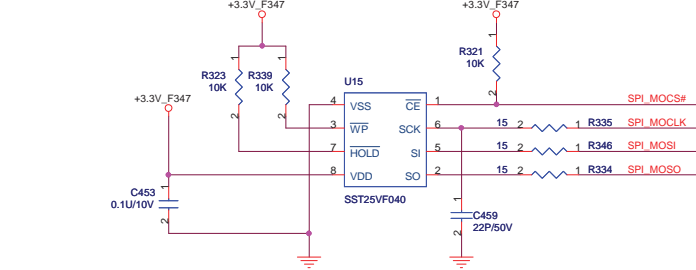
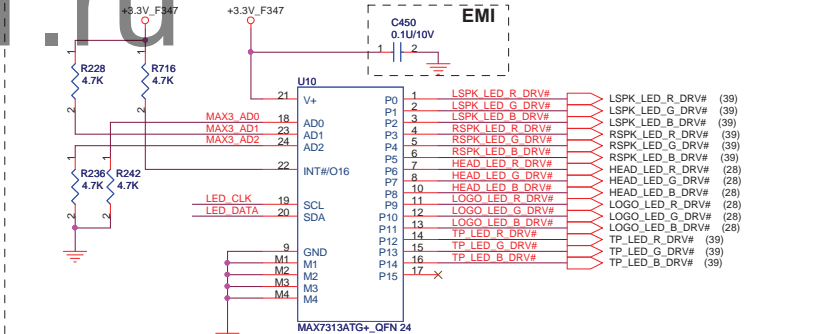
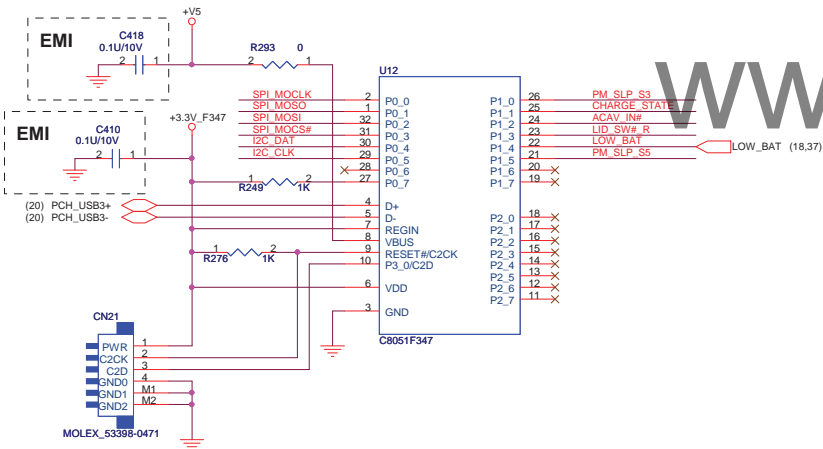
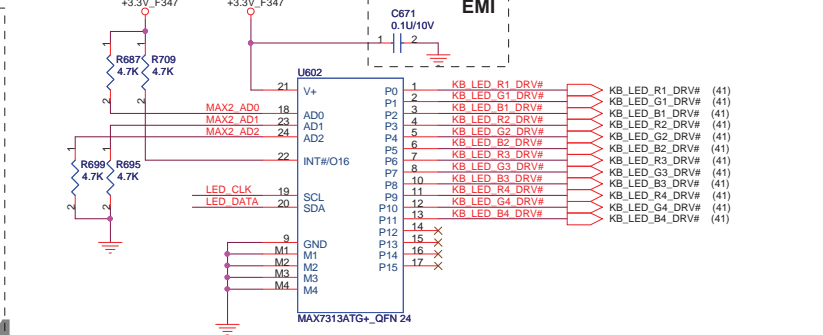
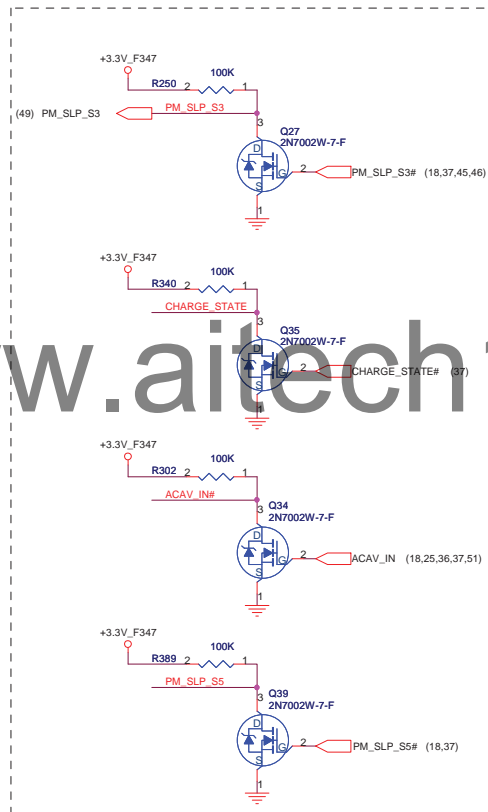
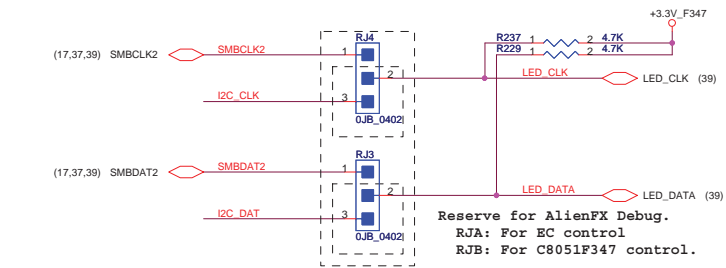
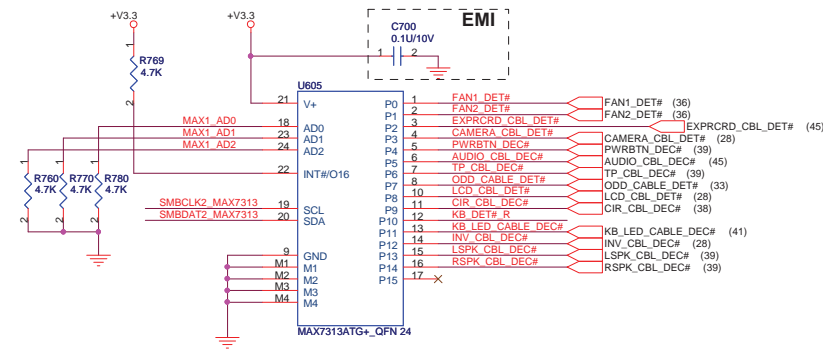
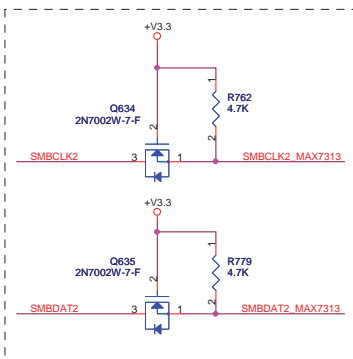
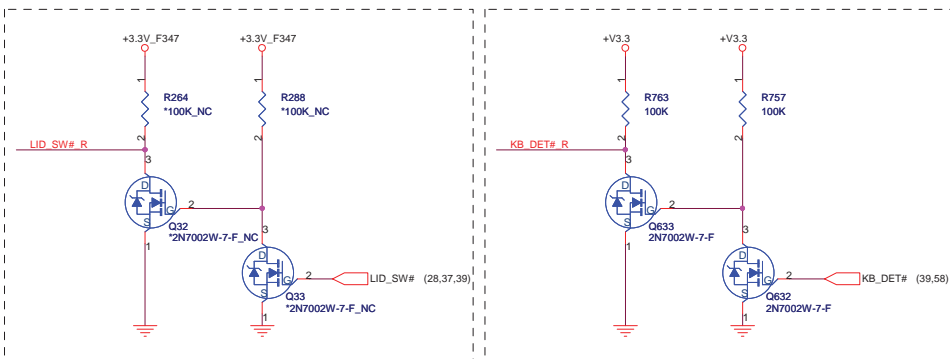
Power Button



8/5 SW600 change mount to NA

Media Board Conn

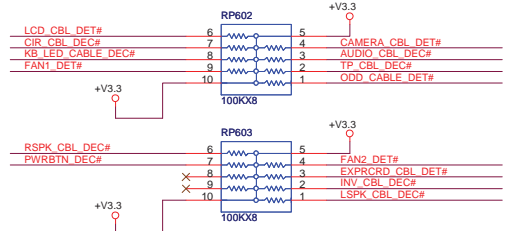
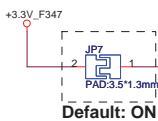




300mA

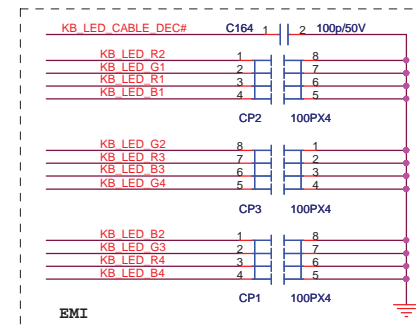
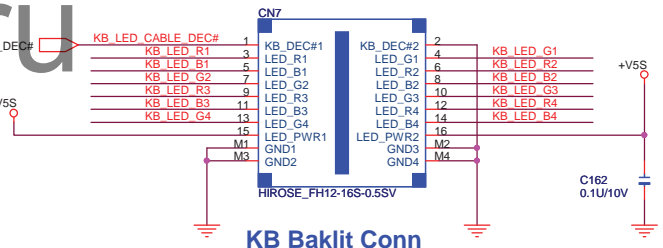
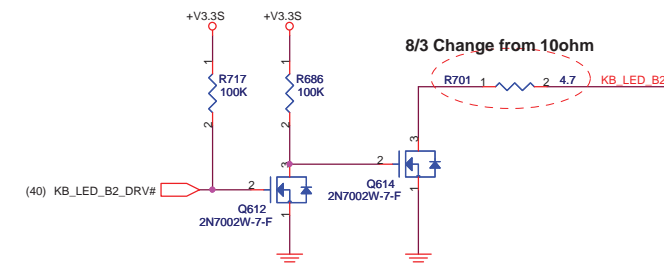
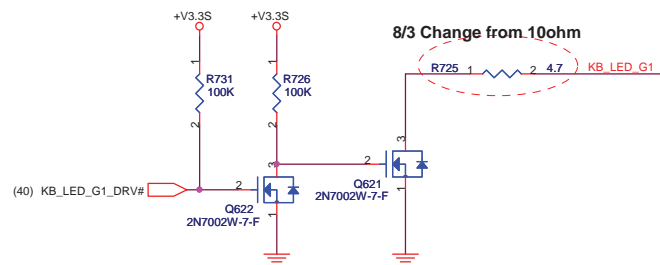
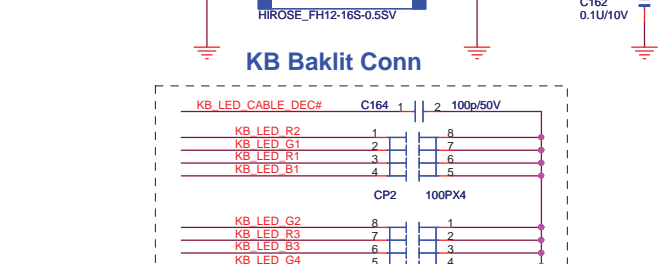
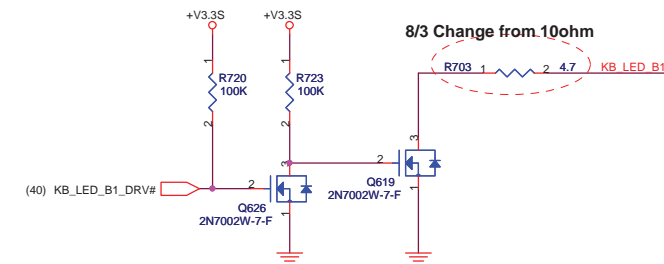
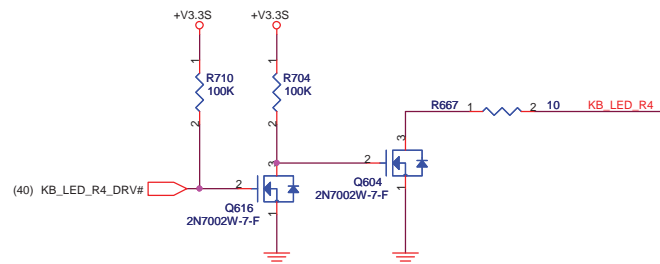
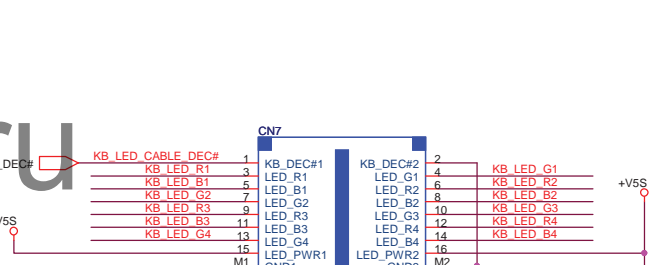
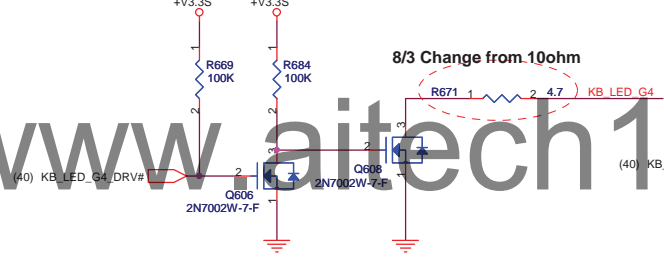
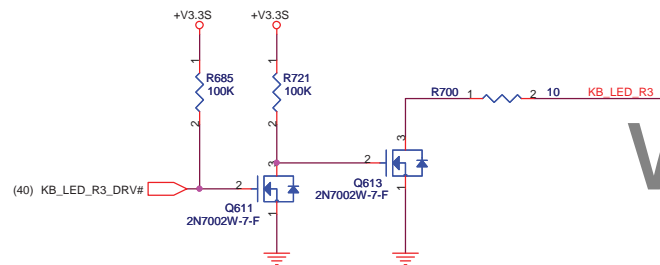
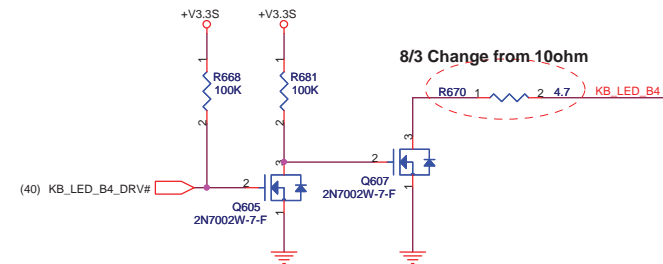
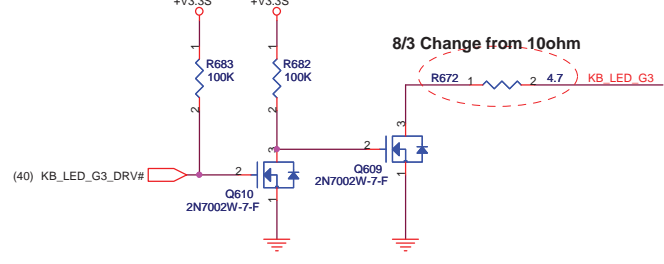
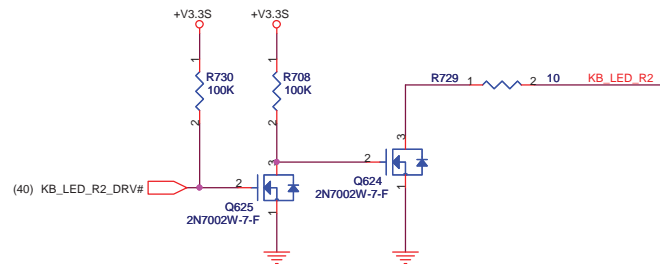
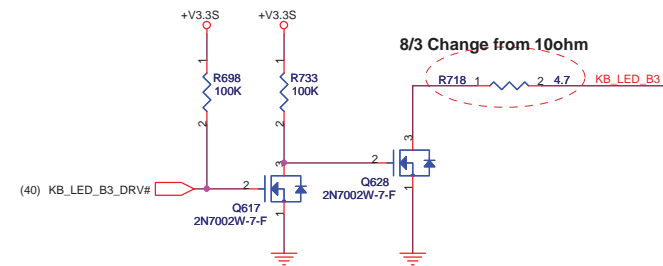
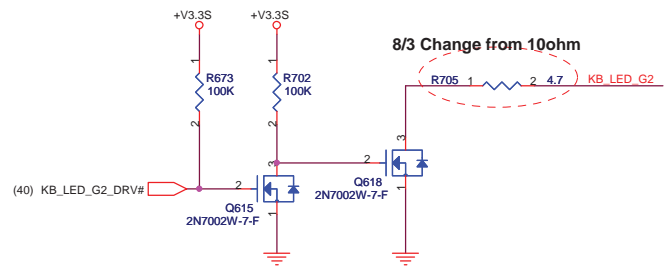
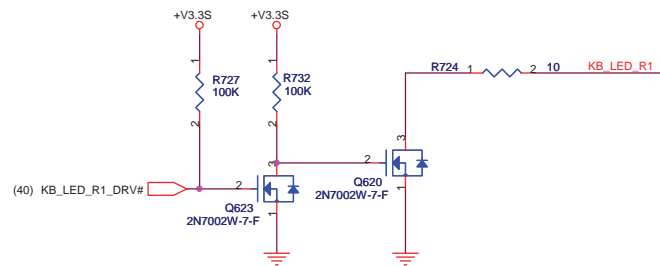
	State			
	S0	S3	S4	S5
AC In	ON	ON	ON	ON
BAT only	ON	ON	Off	Off

300mA

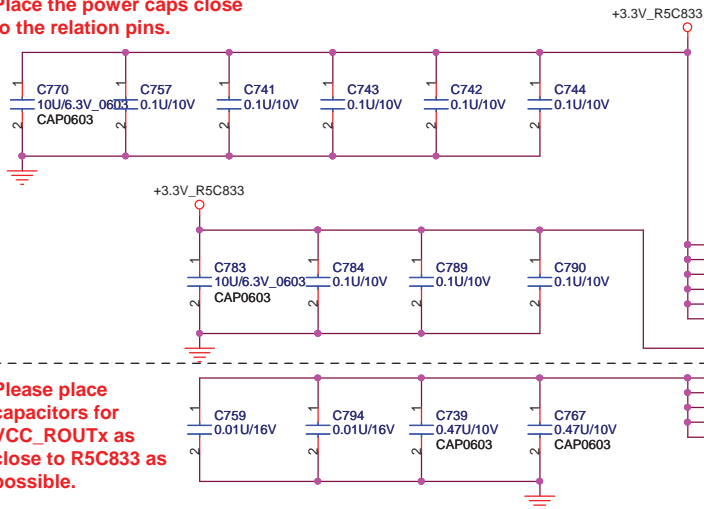


Reference	AD2	AD1	AD0	MAX7313 #
U41	0	0	0	Cable Detect#
U43	0	0	1	KB LED
U45	0	1	0	SPK& Head& Logo& T/P LED
---	0	1	1	LED Board
---	1	0	0	Media Board
---	1	0	1	Media Board

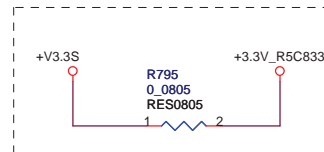
DEVICE	SMBUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM (U40)	1010 000b



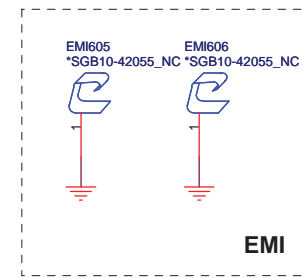
Place the power caps close to the relation pins.



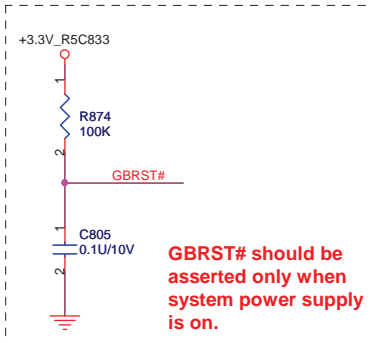
Please place capacitors for VCC_ROUTx as close to R5C833 as possible.



Place the power caps close to the relation pins.



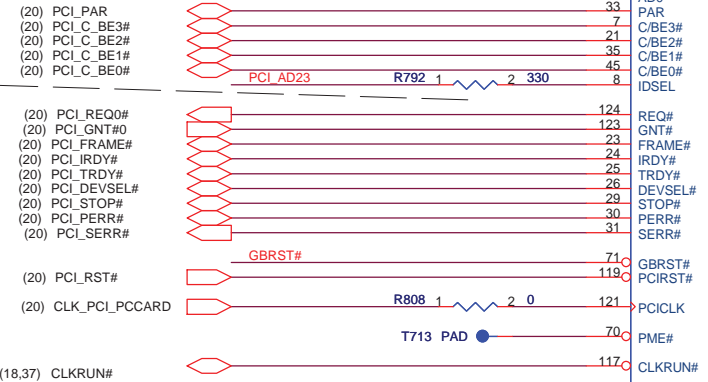
EMI



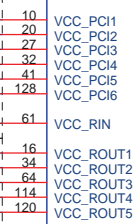
GBRST# should be asserted only when system power supply is on.

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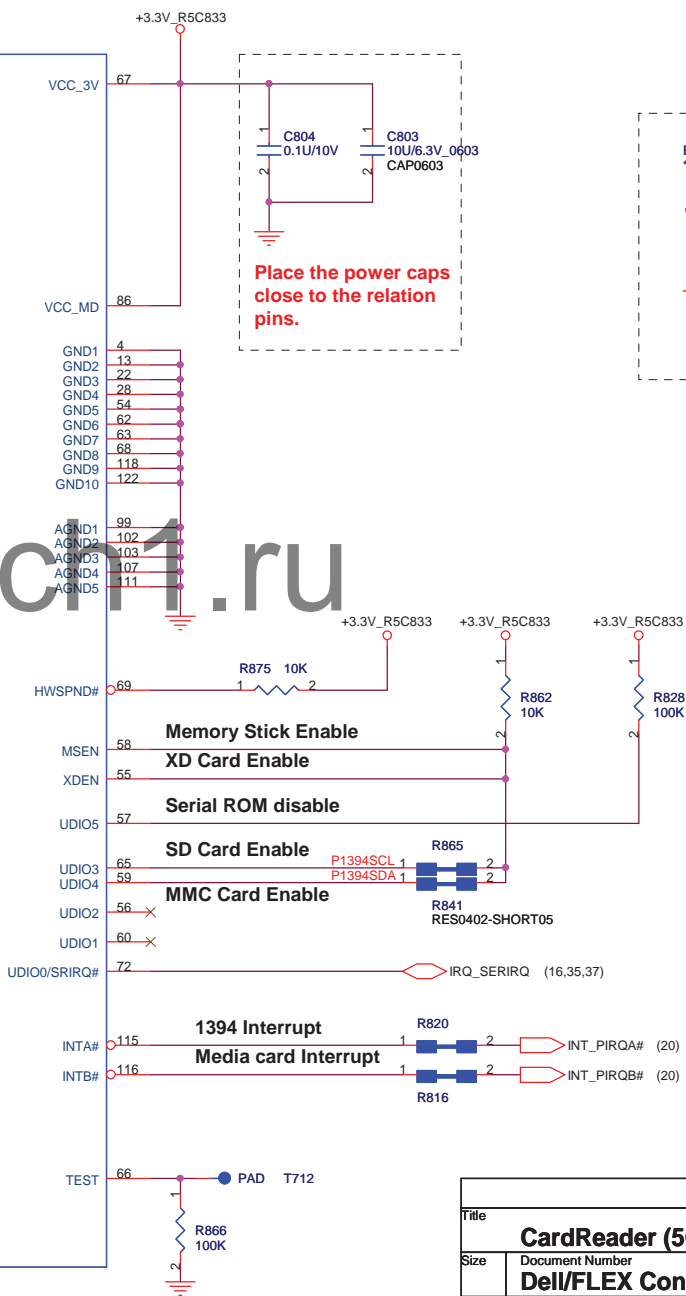
Checklist
300~900ohm



U609B



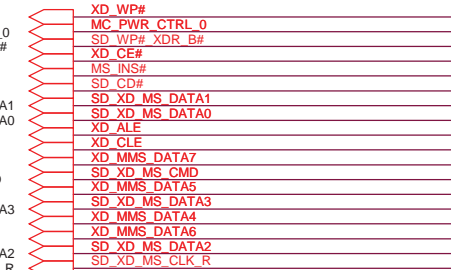
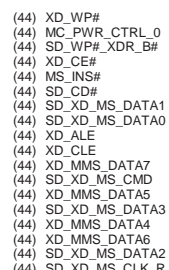
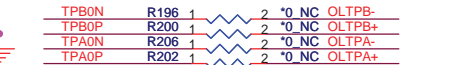
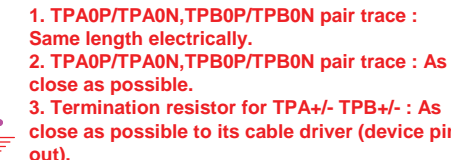
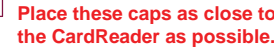
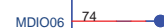
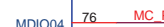
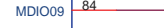
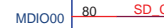
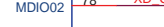
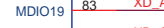
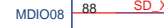
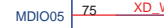
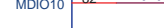
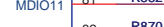
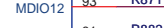
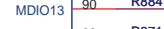
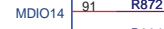
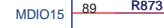
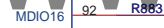
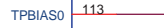
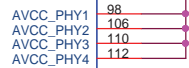
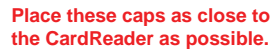
PCI / OTHER



Title CardReader (5C833)		
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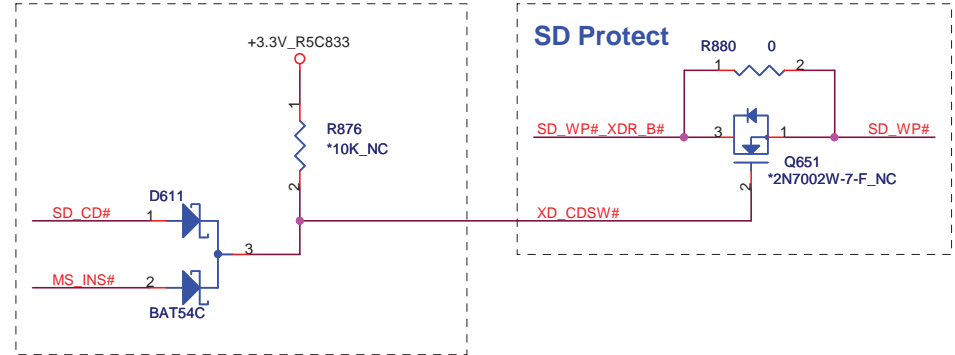
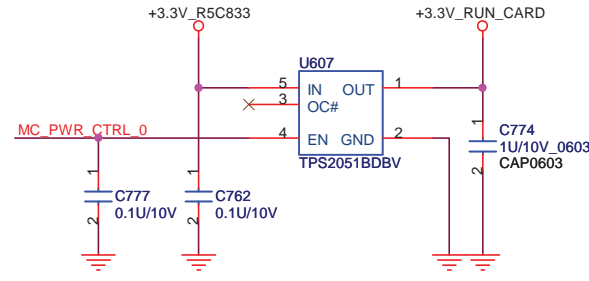


**XTAL for XO/XI, 50ppm or better
Required**



Layout Note:

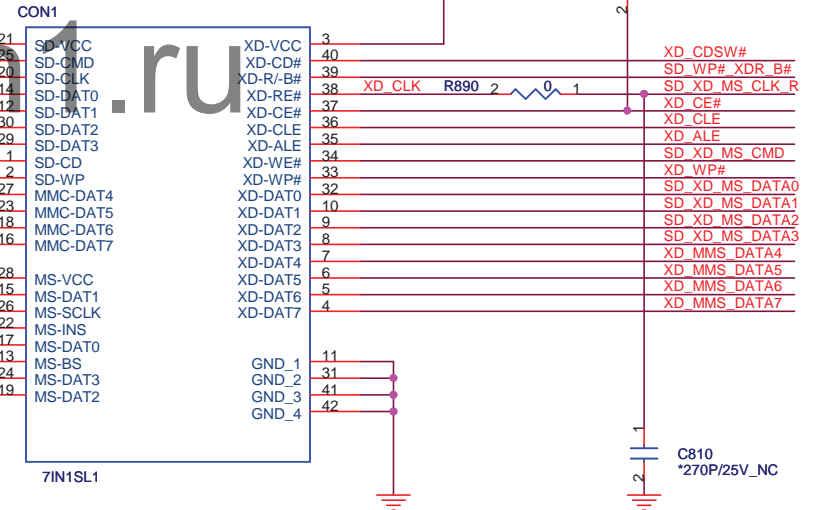
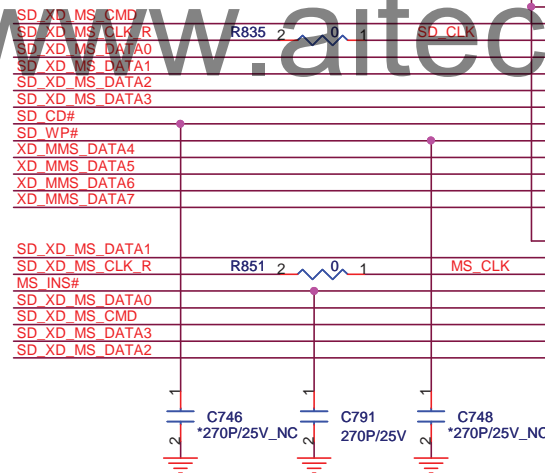
- 1). The distance between Media Card Power Switch and Media Socket should be less than 2-inches.
- 2). The trace width for +3.3V_RUN_CARD should be 40MIL at least.
- 3). The GND trace for Media Card Socket should be 40MIL at least.



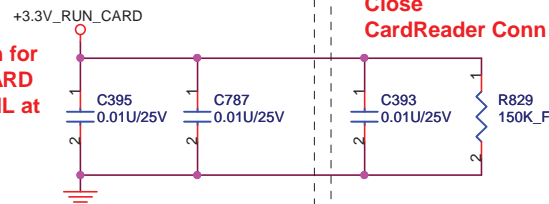
2.2uF cap is no more than 250mils away from the power pin and a have a min trace width of 40mils.

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(43) XD_WP#	XD_WP#
(43) MC_PWR_CTRL_0	MC_PWR_CTRL_0
(43) SD_WP#_XDR_B#	SD_WP#_XDR_B#
(43) XD_CE#	XD_CE#
(43) MS_INS#	MS_INS#
(43) SD_CD#	SD_CD#
(43) SD_XD_MS_DATA1	SD_XD_MS_DATA1
(43) SD_XD_MS_DATA0	SD_XD_MS_DATA0
(43) XD_ALE	XD_ALE
(43) XD_CLE	XD_CLE
(43) XD_MMS_DATA7	XD_MMS_DATA7
(43) SD_XD_MS_CMD	SD_XD_MS_CMD
(43) XD_MMS_DATA5	XD_MMS_DATA5
(43) SD_XD_MS_DATA3	SD_XD_MS_DATA3
(43) XD_MMS_DATA4	XD_MMS_DATA4
(43) XD_MMS_DATA6	XD_MMS_DATA6
(43) SD_XD_MS_DATA2	SD_XD_MS_DATA2
(43) SD_XD_MS_CLK_R	SD_XD_MS_CLK_R



The trace width for +3.3V_RUN_CARD should be 40MIL at least.

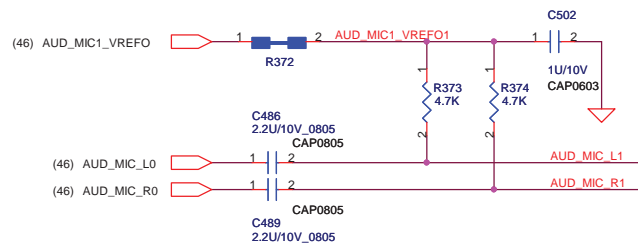
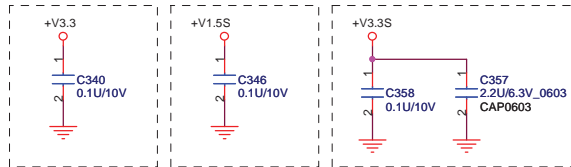
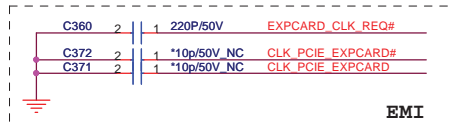
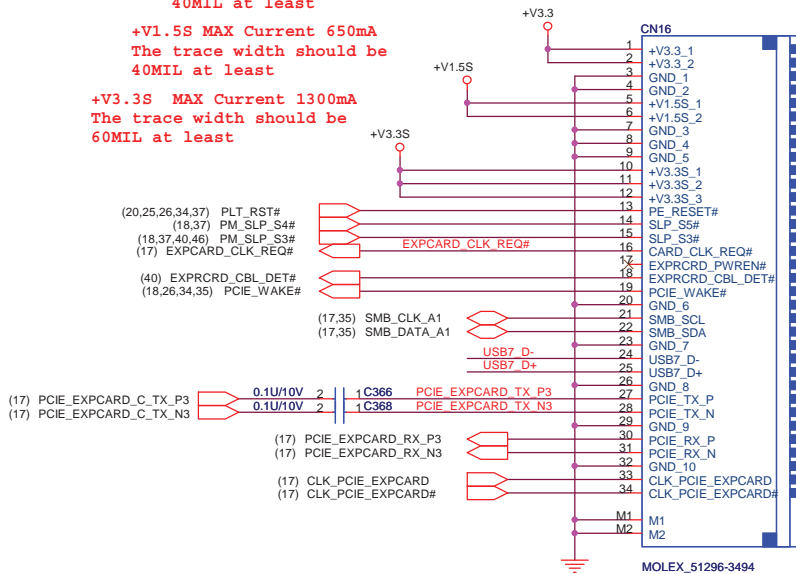


Title		
CardReader CONN		
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+V3.3 MAX Current 275mA
The trace width should be
40MIL at least

+V1.5S MAX Current 650mA
The trace width should be
40MIL at least

+V3.3S MAX Current 1300mA
The trace width should be
60MIL at least



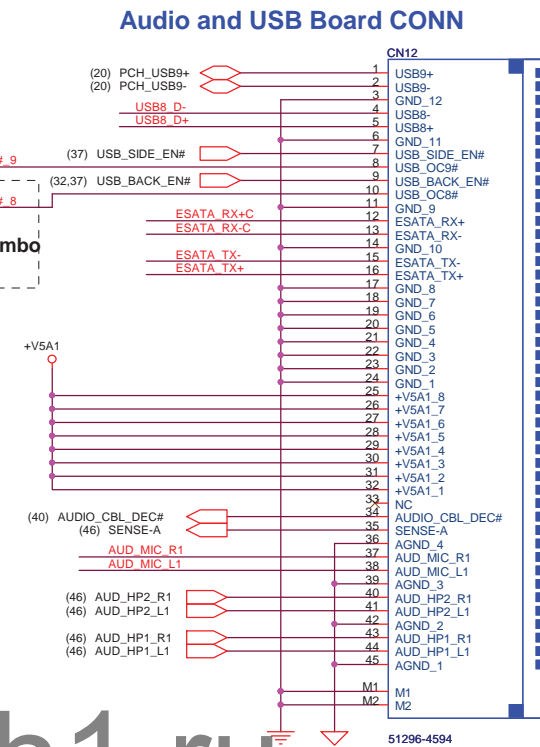
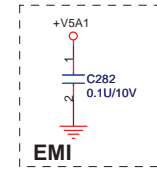
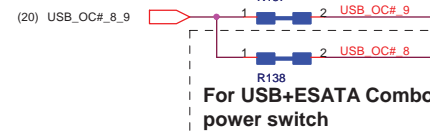
(20) PCH_USB7+
(20) PCH_USB7-

USB7 D+
USB7 D-

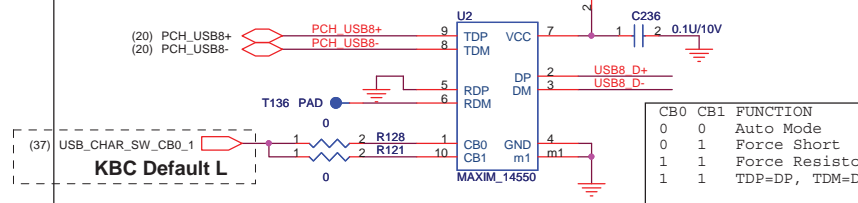
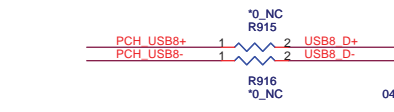
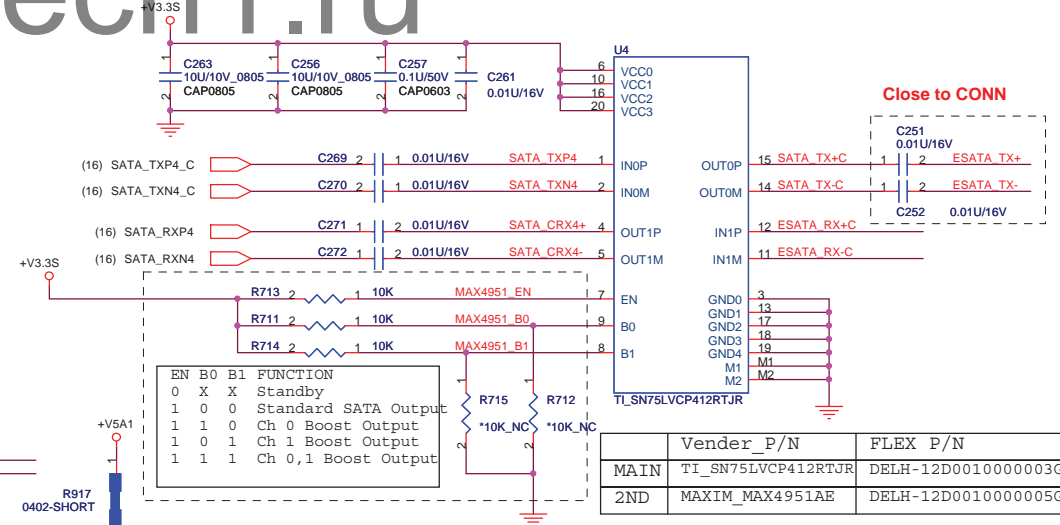
*DLW21SN900SQ2B_NC

R190 0
1 2

R189 0
1 2



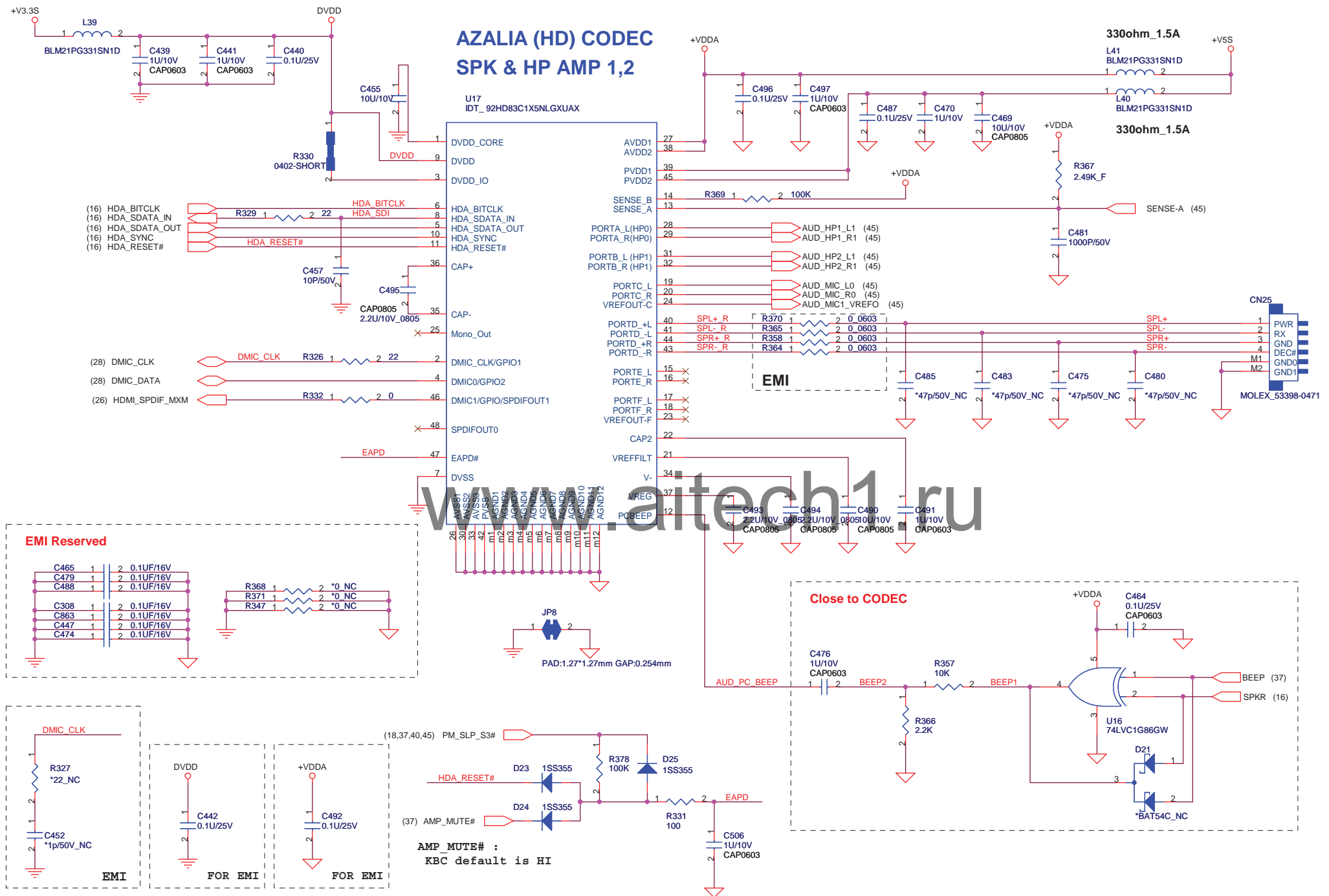
For eSATA/USB CONN



	Vender_P/N	FLEX P/N
MAIN	TI_SN75LVCP412RTJR	DELH-12D0010000003G
2ND	MAXIM_MAX4951AE	DELH-12D0010000005G

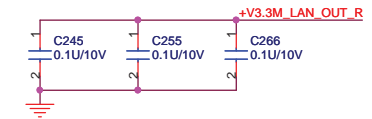
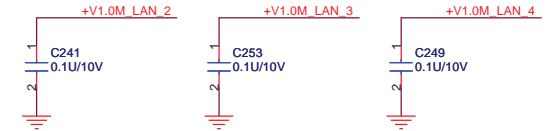
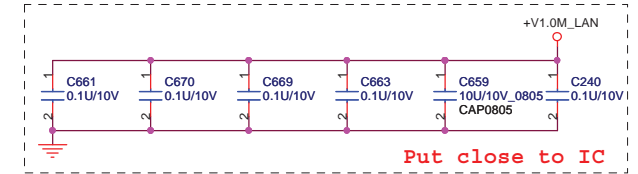
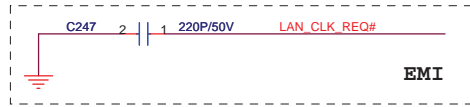
Title			
Audio/B Exp/B CONN			
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AZALIA (HD) CODEC SPK & HP AMP 1,2

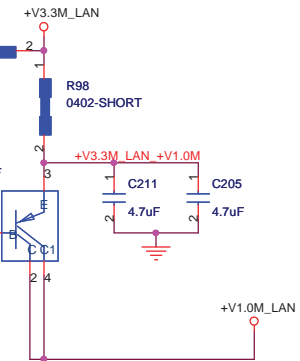
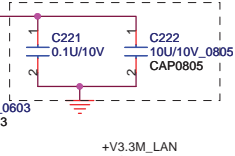


Title			Audio (92HD83)/CONN		
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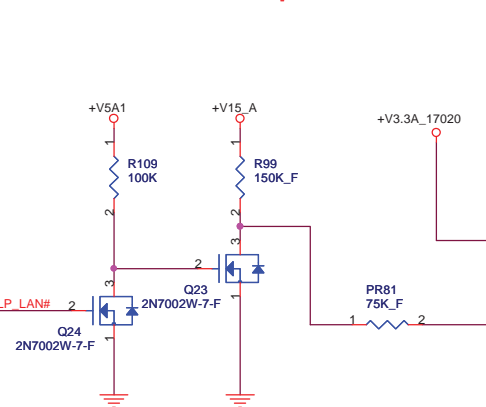
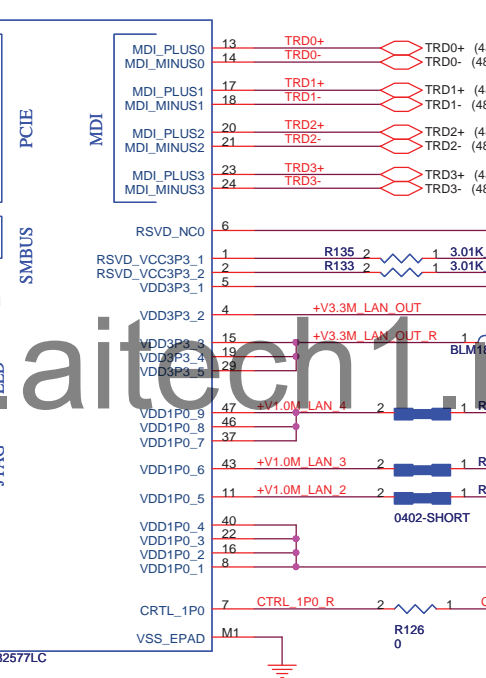
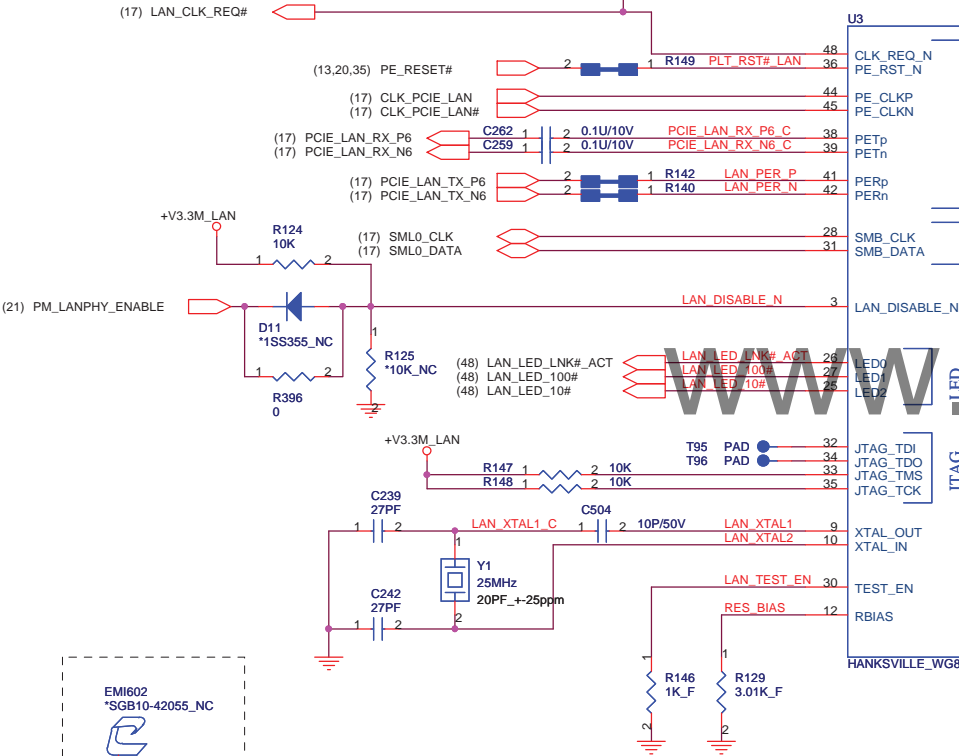
Hanksville PHY	FLEX P/N
WG82577LC QLMH A3	DELH-10D0040000005G



Near pin 1&2



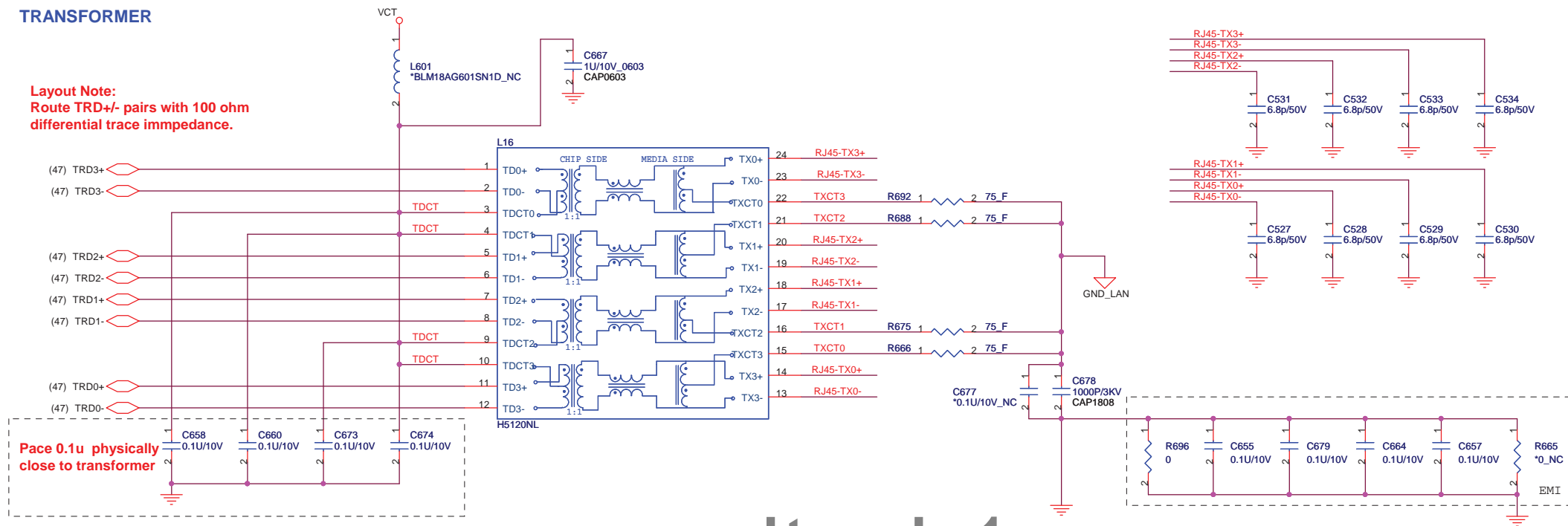
+V3.3M_LAN (17,22,48,49)



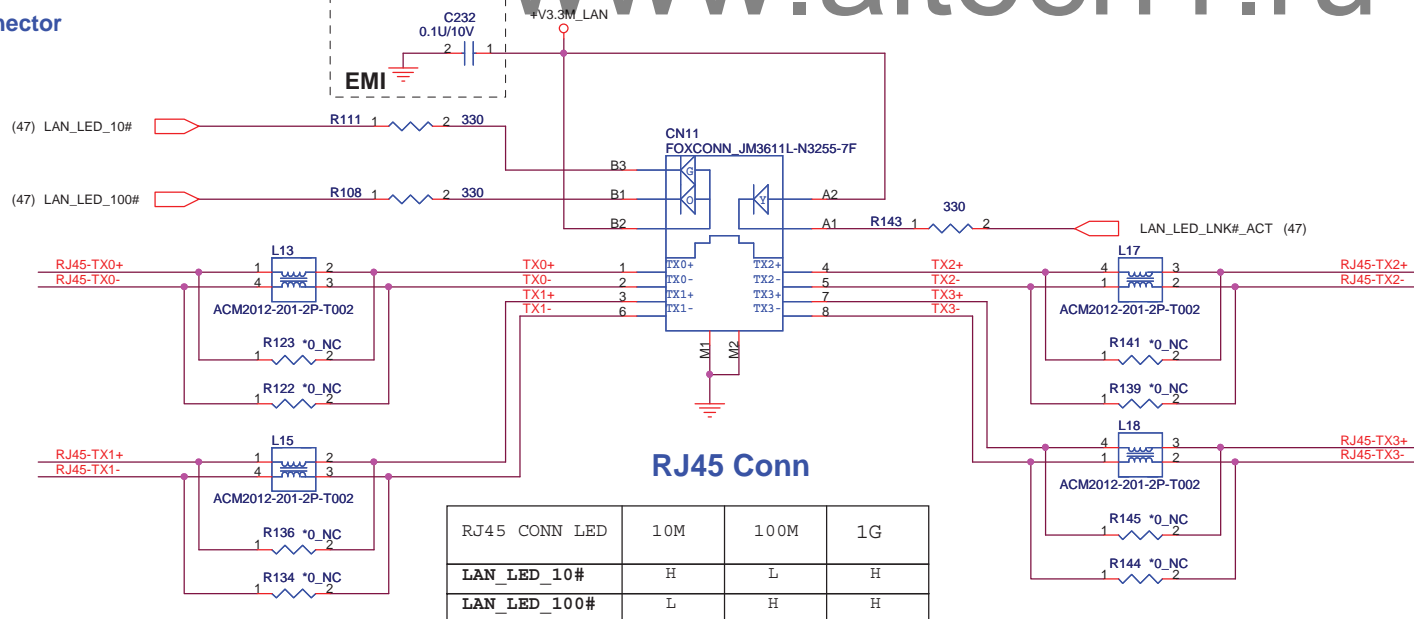
Title	PHY_HANKSVILLE GbE LAN		
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TRANSFORMER

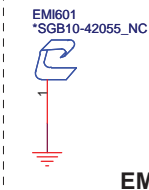
Layout Note:
Route TRD+/- pairs with 100 ohm differential trace impedance.



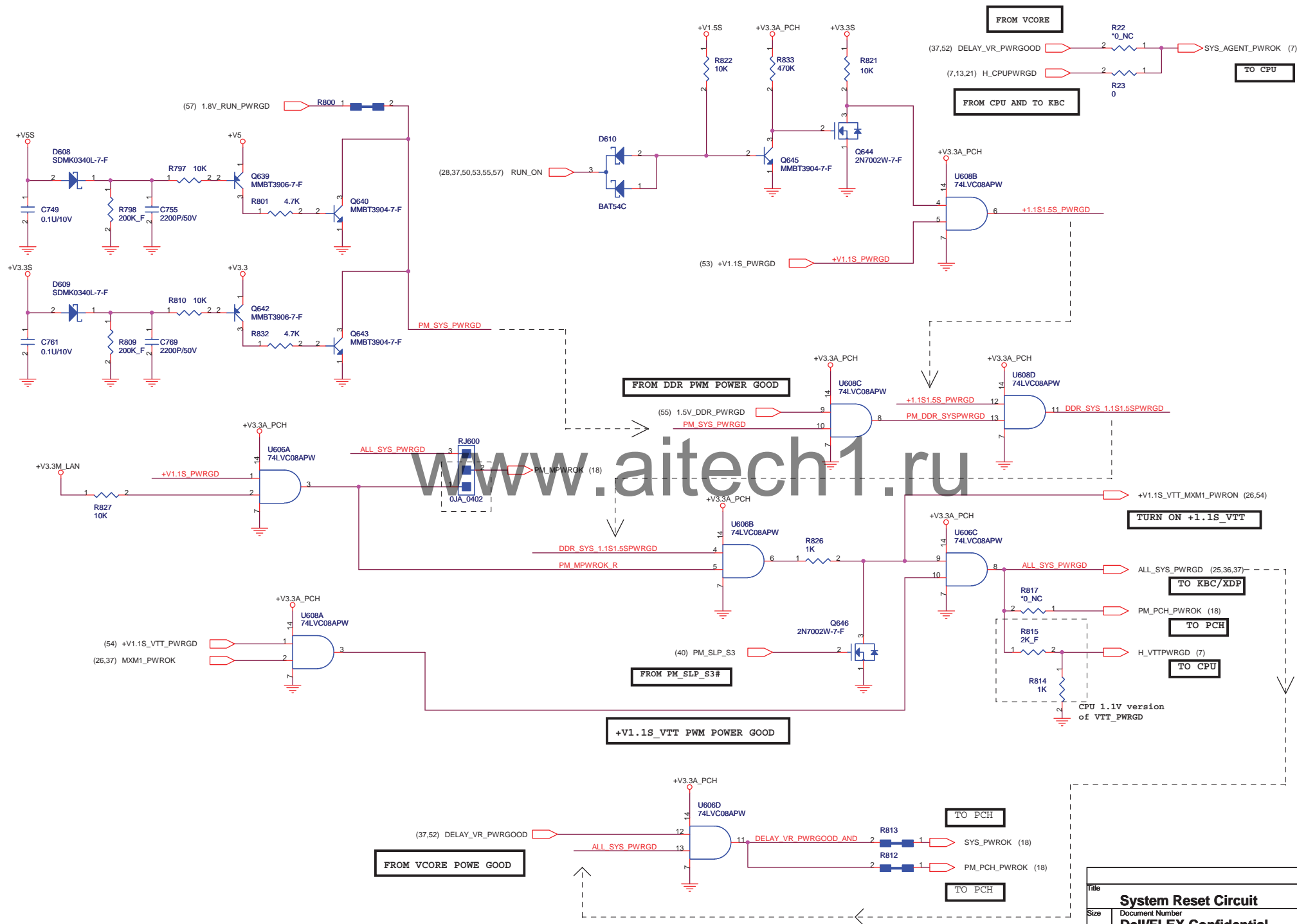
RJ-45 Connector

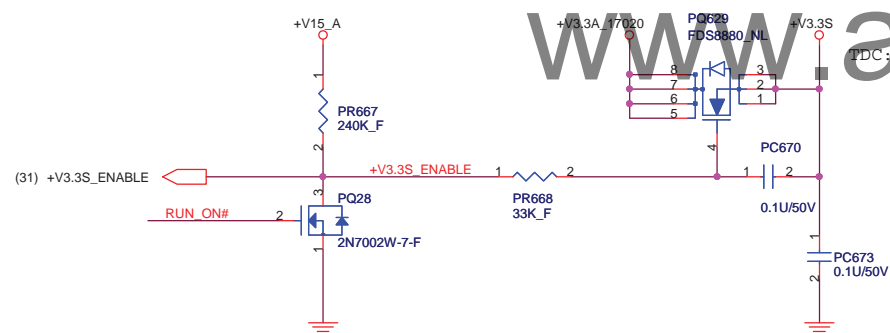
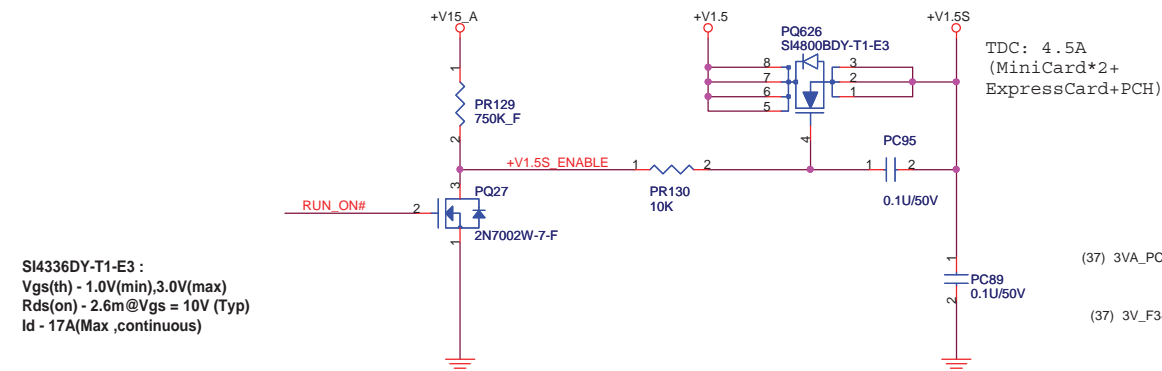
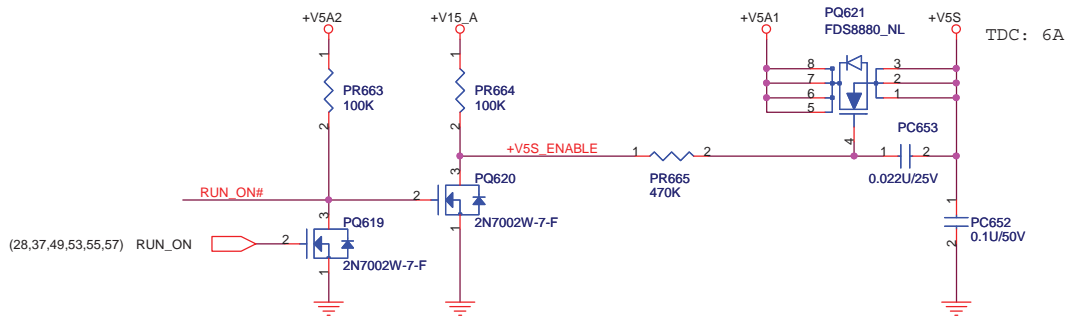


RJ45 CONN LED	10M	100M	1G
LAN_LED_10#	H	L	H
LAN_LED_100#	L	H	H

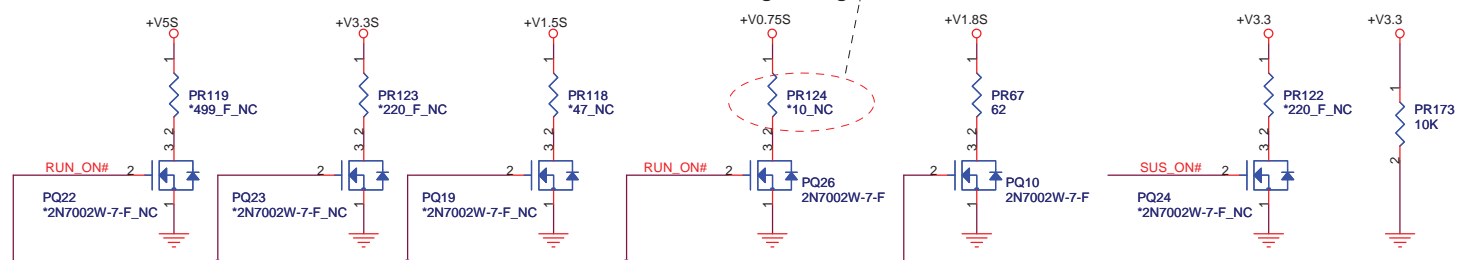


Title		
RJ-45/TRANSFORM		
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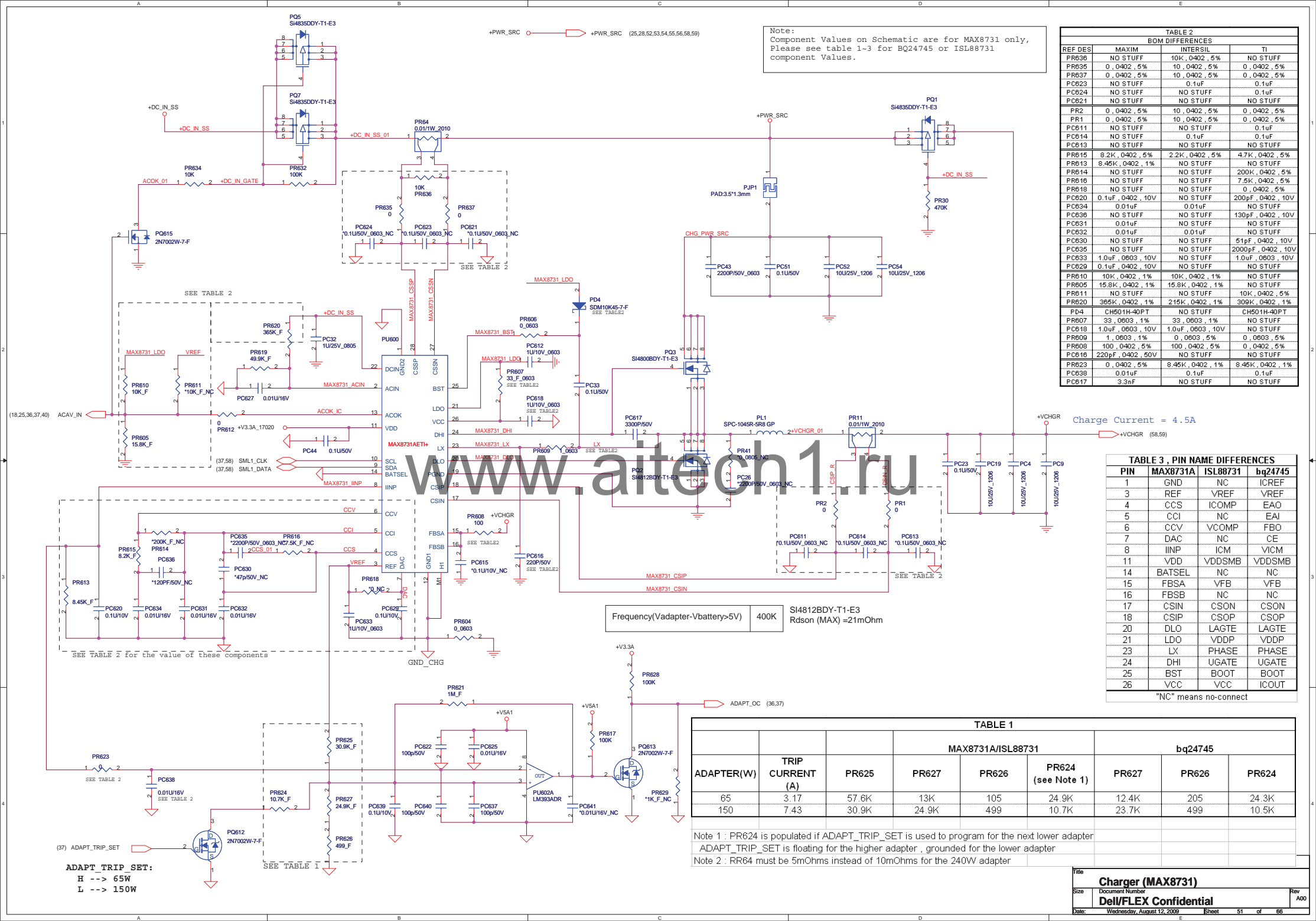


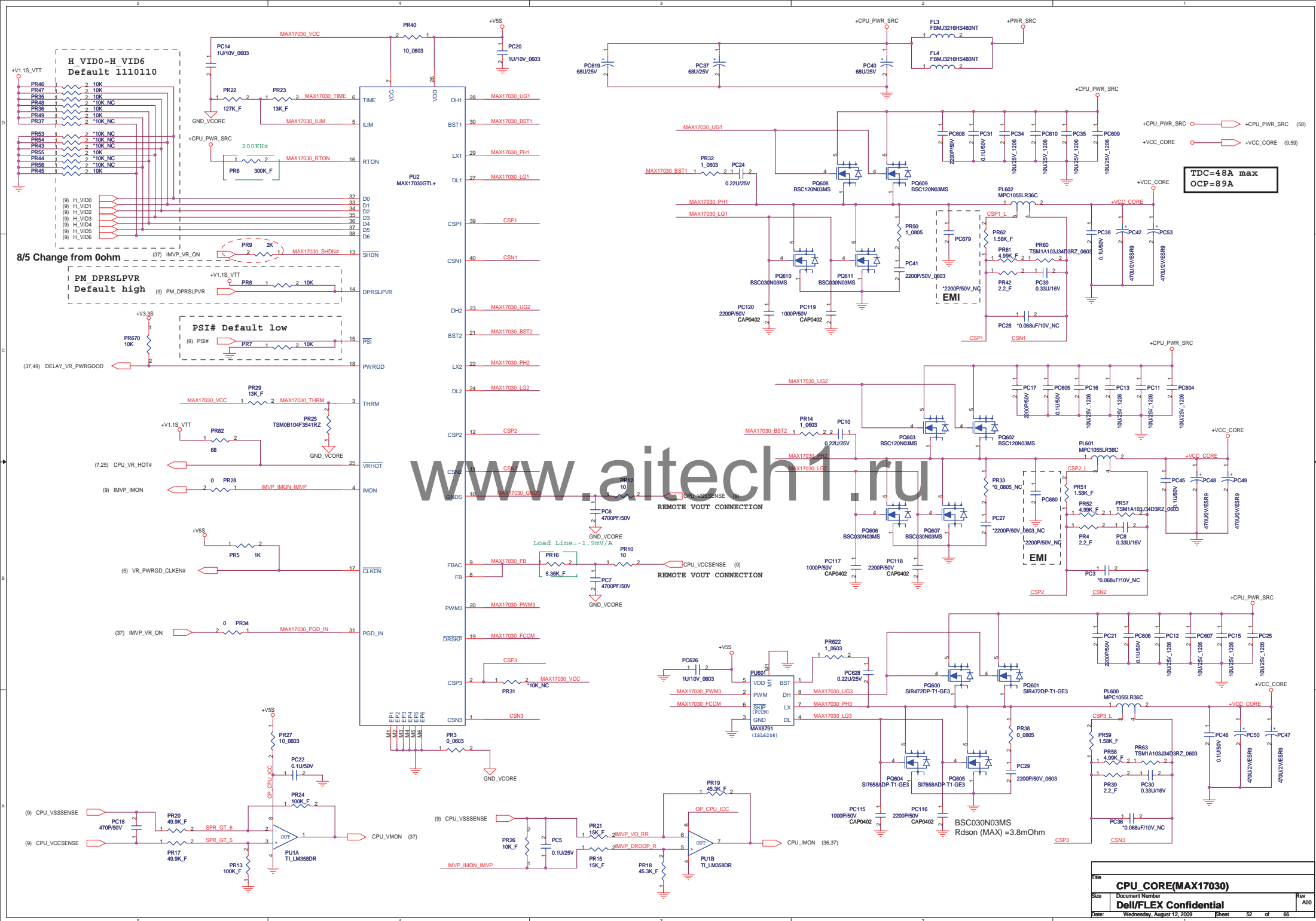


FDS8880_NL : Vgs(th) - 1.2V(min),2.5V(max)
Rds(on) - 7.9m@Vgs = 10V (Typ)
Id - 11.6A(Max ,continuous)

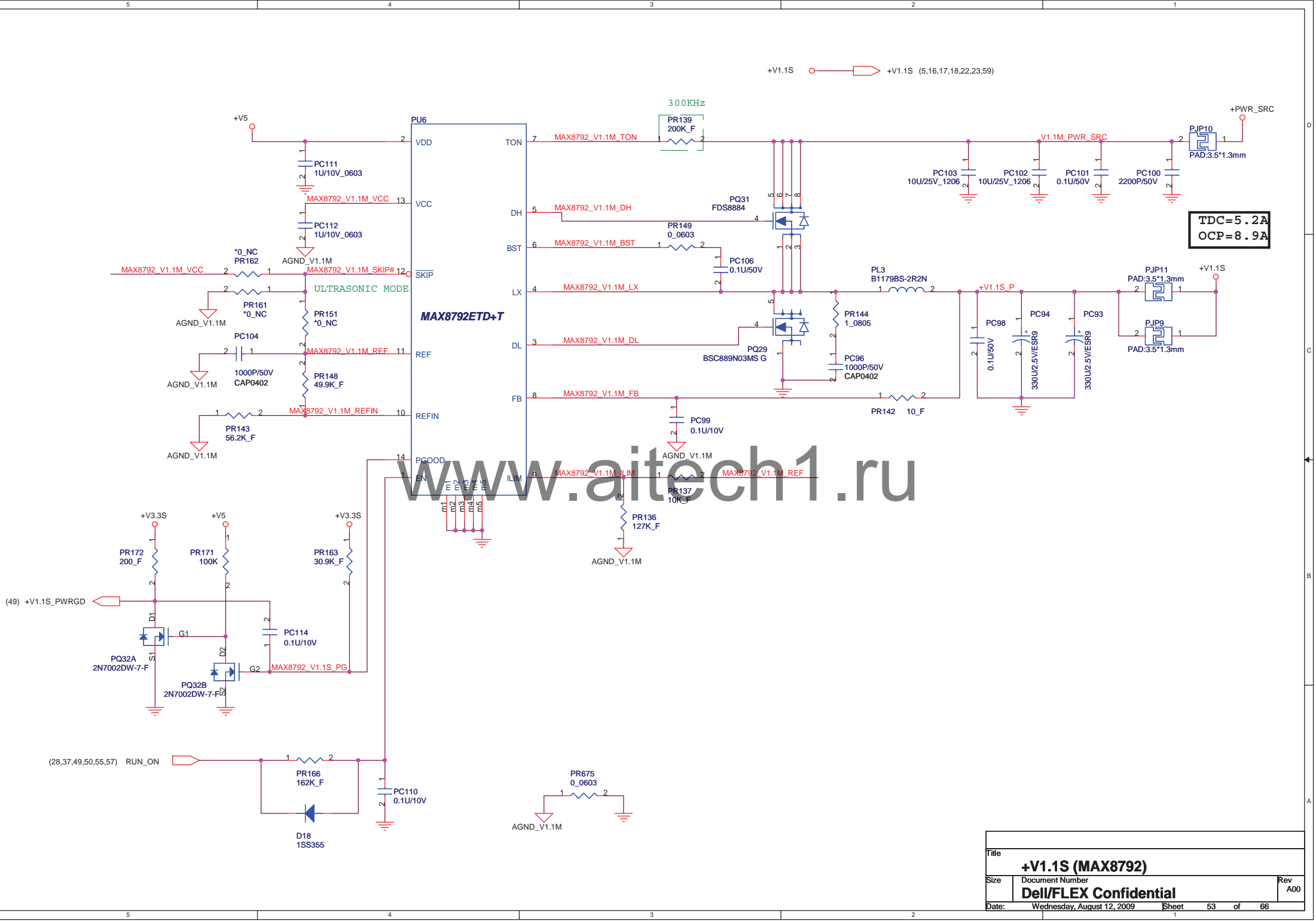


Title			
SUS/ RUN POWER SW			
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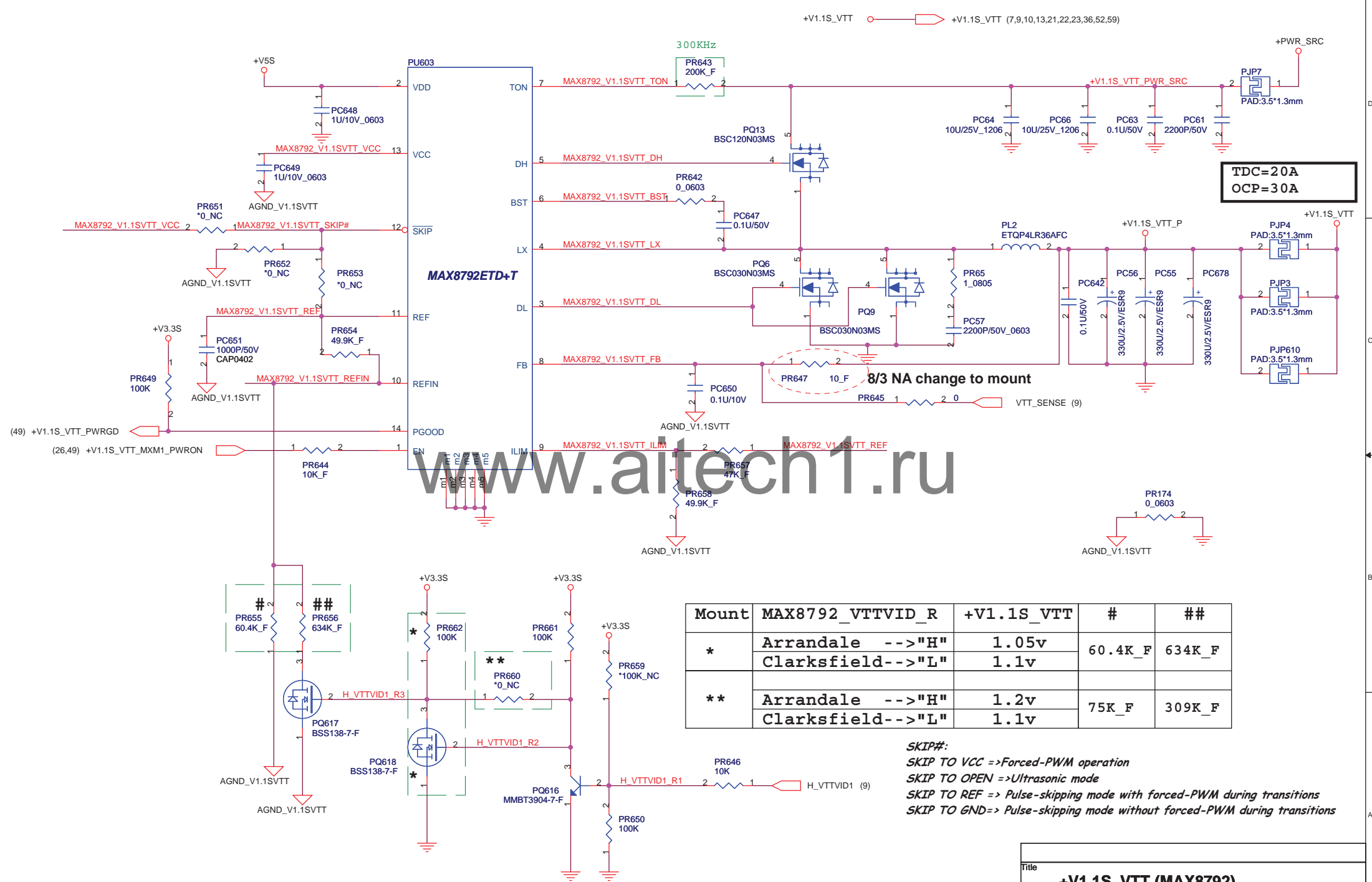


Title			CPU_CORE(MAX17030)
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TDC=5.2A
OCP=8.9A

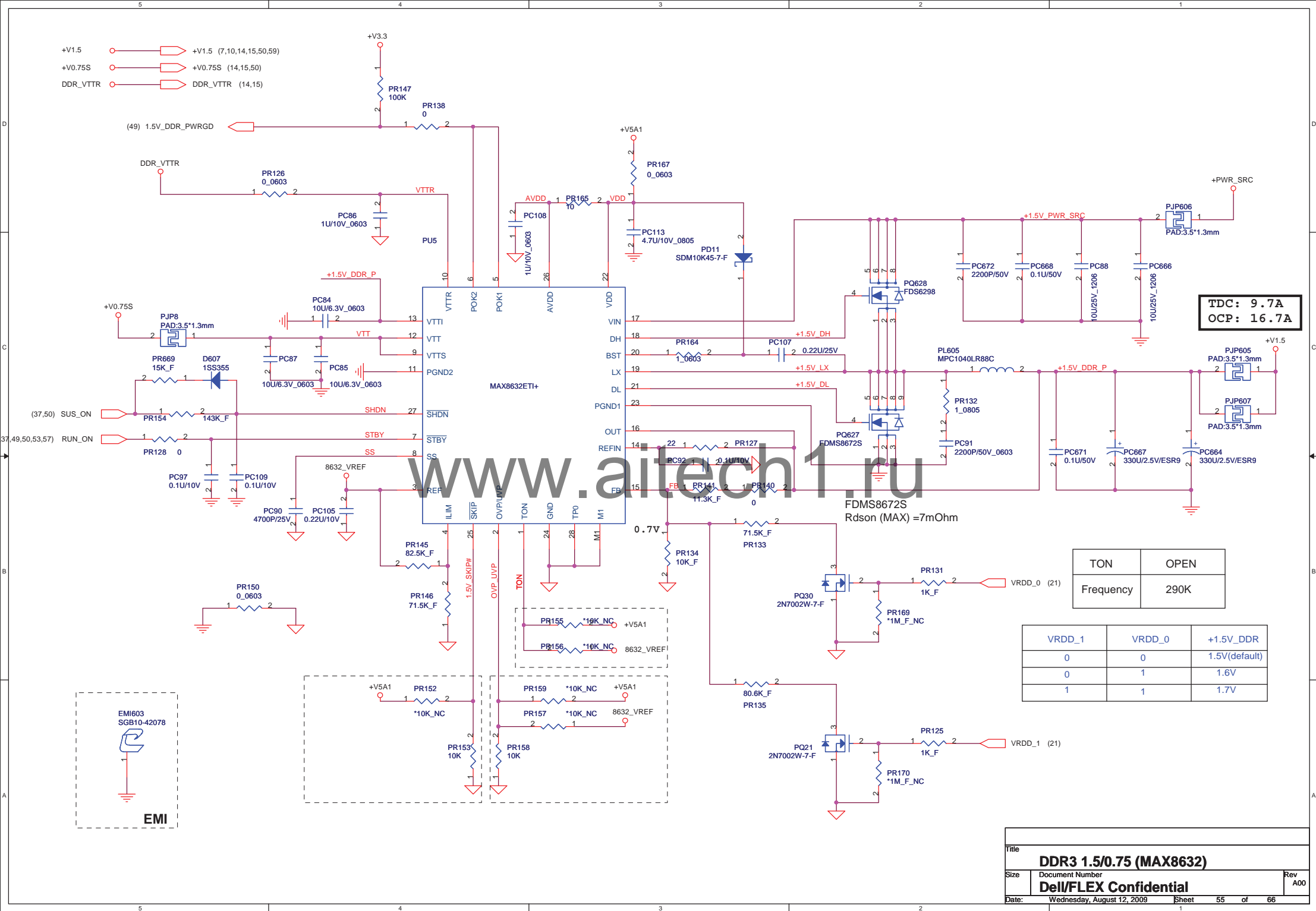
Title		
+V1.1S (MAX8792)		
Size	Document Number	Rev
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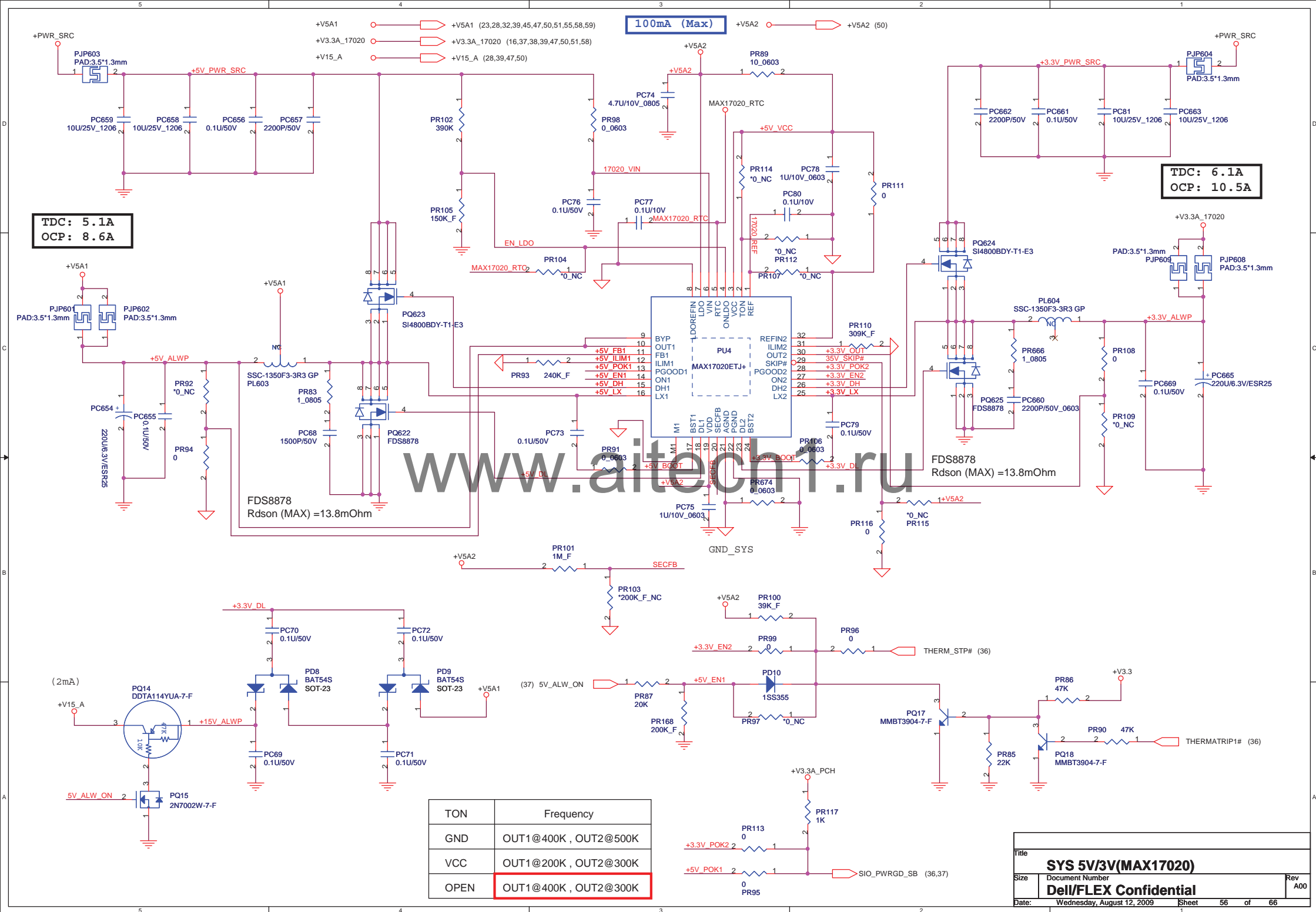


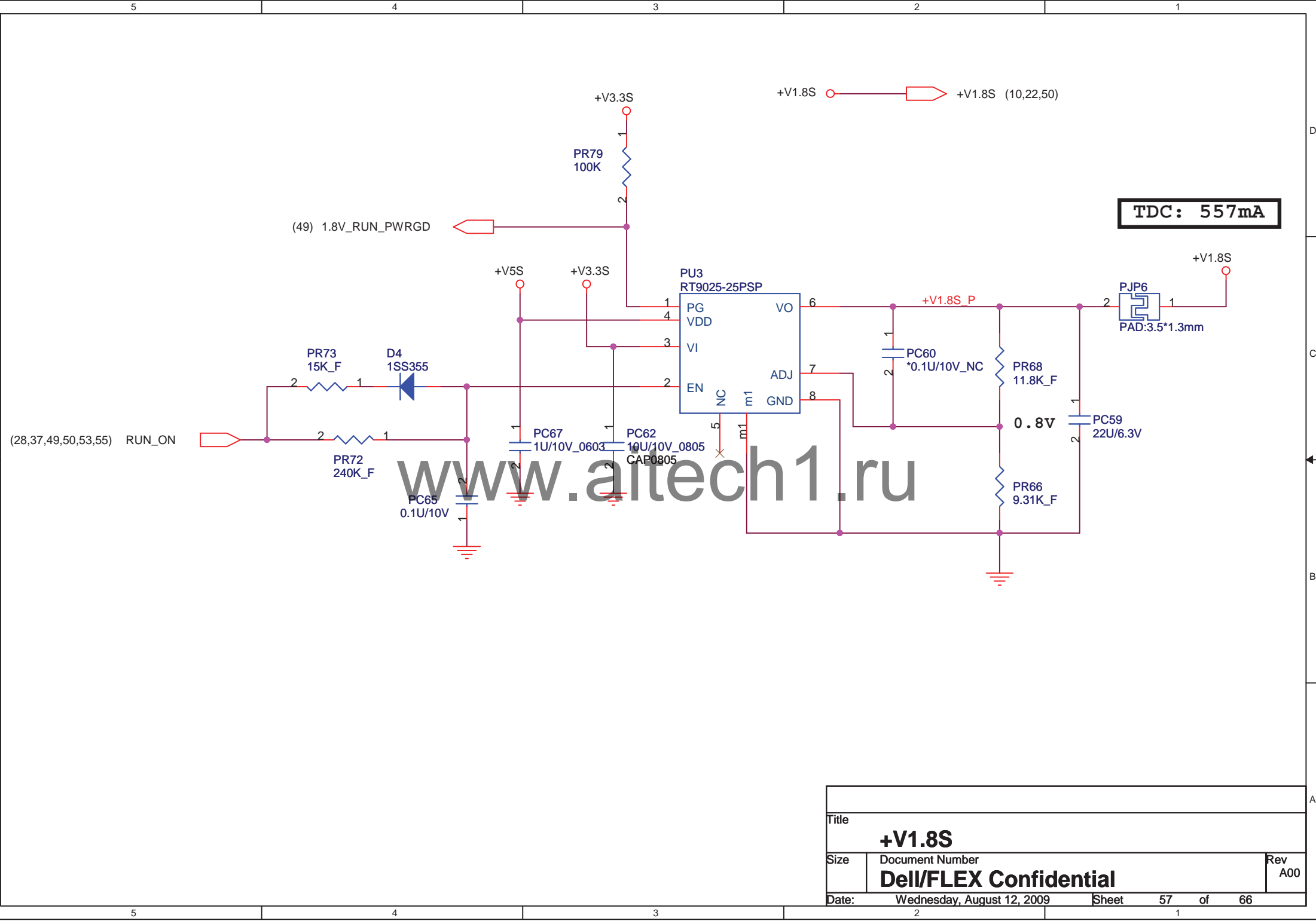
TDC=20A
OCP=30A

Mount	MAX8792_VTTVID_R	+V1.1S_VTT	#	##
*	Arrandale -->"H"	1.05v	60.4K_F	634K_F
	Clarksfield-->"L"	1.1v		
**	Arrandale -->"H"	1.2v	75K_F	309K_F
	Clarksfield-->"L"	1.1v		

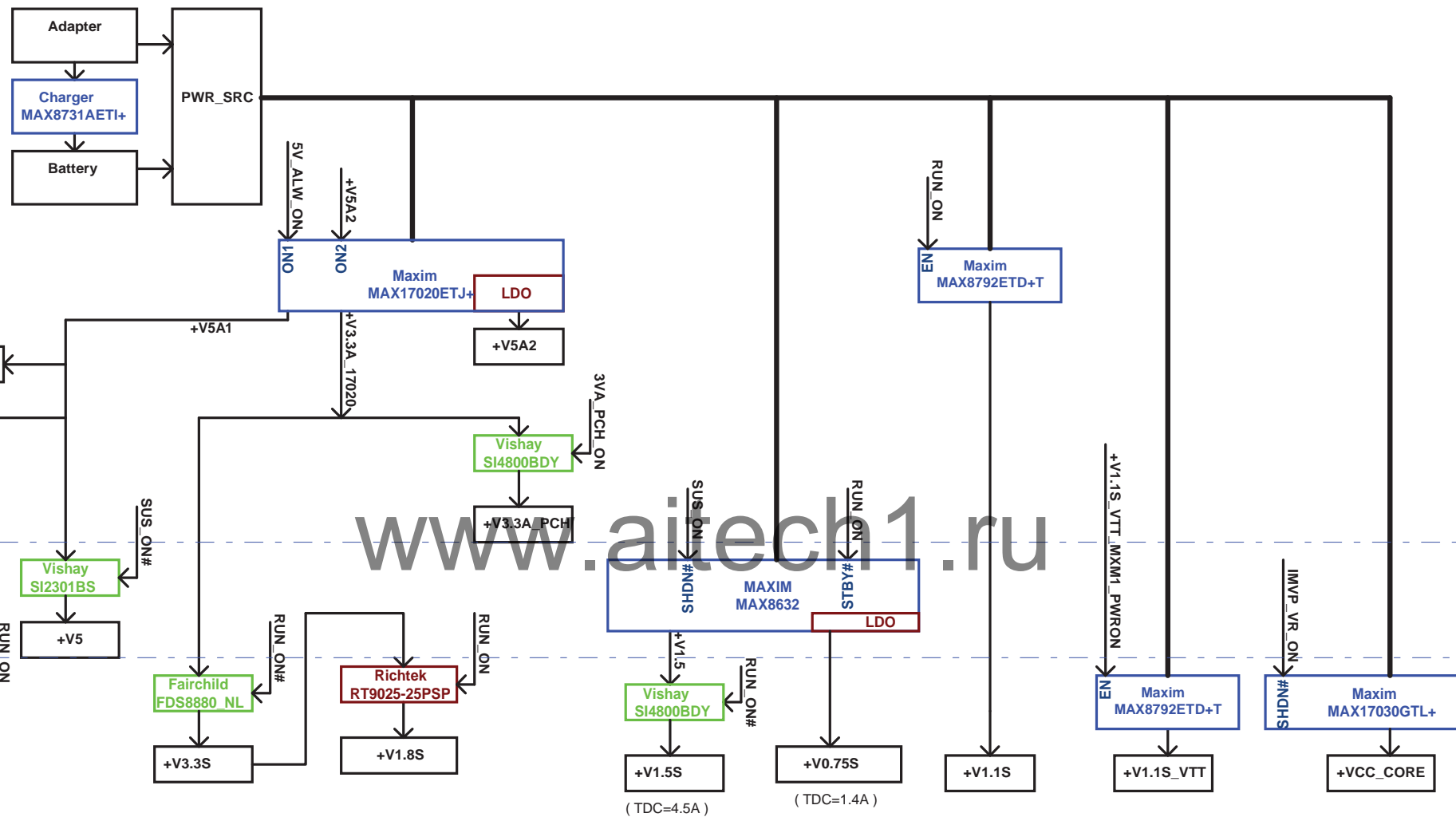
SKIP#:
SKIP TO VCC => Forced-PWM operation
SKIP TO OPEN => Ultrasonic mode
SKIP TO REF => Pulse-skipping mode with forced-PWM during transitions
SKIP TO GND=> Pulse-skipping mode without forced-PWM during transitions







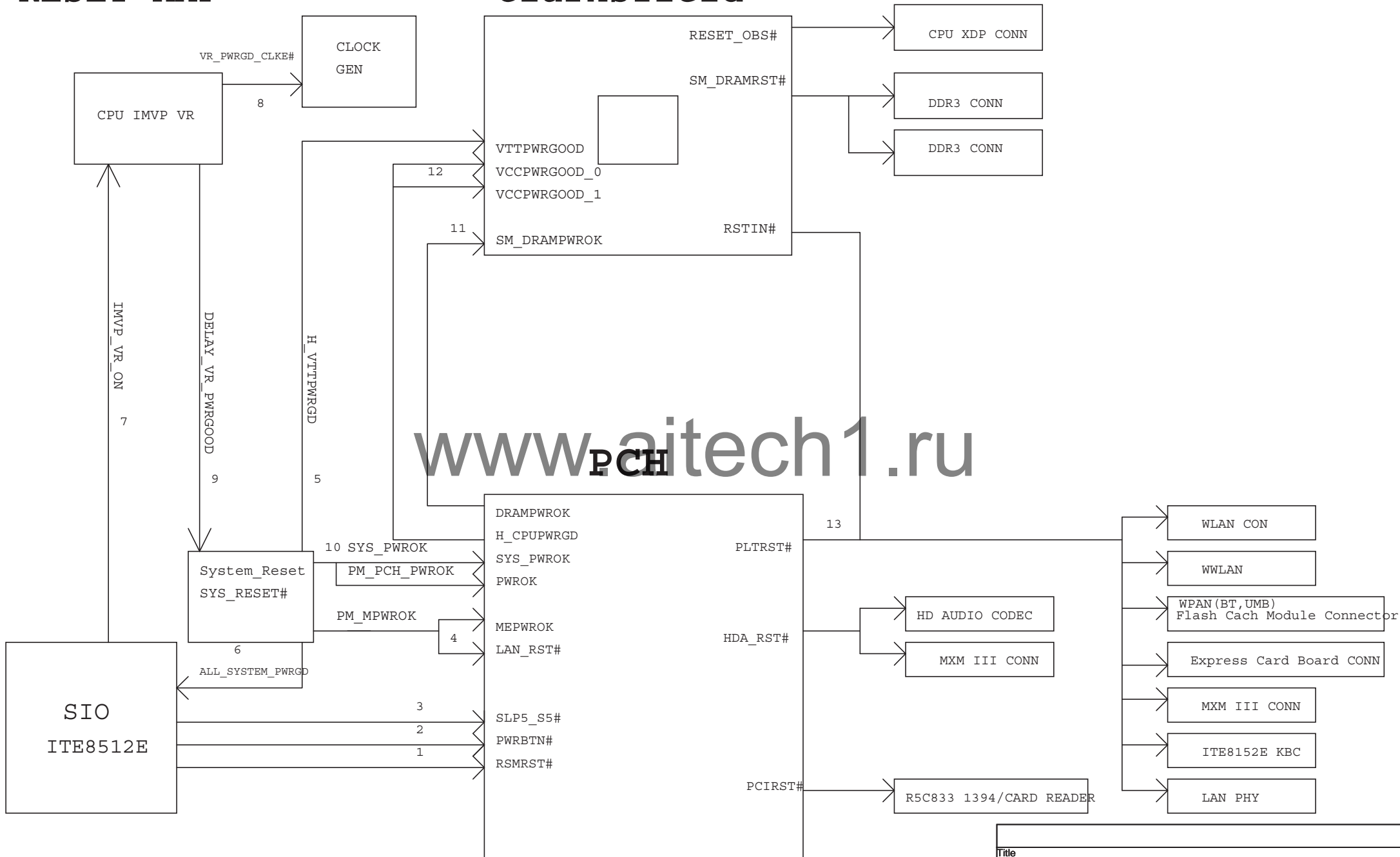
Title				
+V1.8S				
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Power Rail	+V5A1	+V5A2	+V15_A	+V3.3A_17020	+V1.8S	+V1.5	+V0.75S	+V1.1S	+V1.1S_VTT	+VCC_CORE
TDC (Thermal Design Current)	5.1A	100mA	2mA	6.1A	557mA	9.7A	1.4A	5.2A	15A	65A
OCF (Over Current Protect)	8.6A	260mA		10.5A	2A	16.7A	5A	8.9A	25.32A	89A

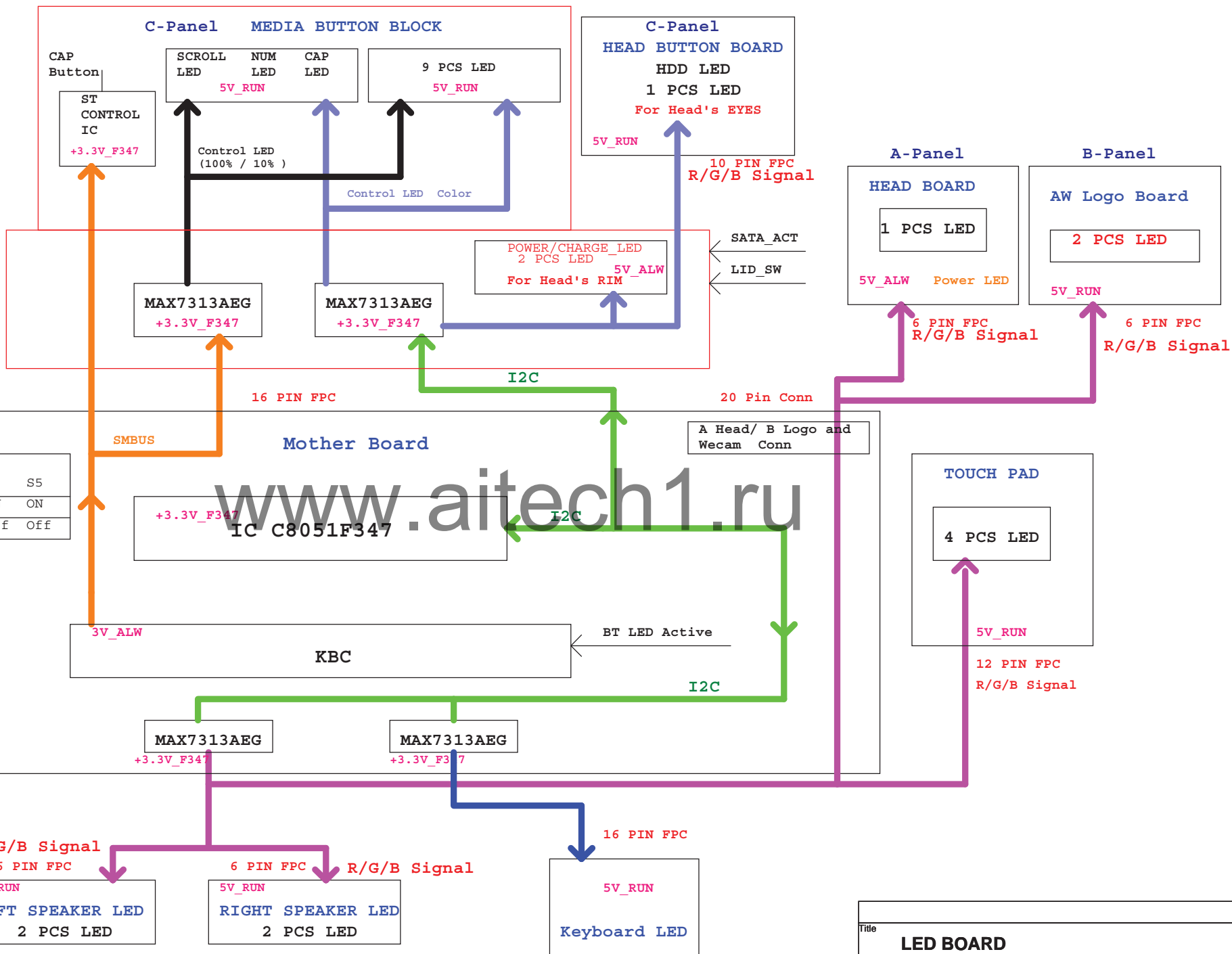
RESET MAP

Clarksfield



Title		
RESET MAP		
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Media button board
 1. Play/Pause
 2. Stop
 3. Skip Back
 4. Skip Forward
 5. Vol_DWN
 6. Vol_UP
 7. Wireless On/Off
 8. AW Command
 9. Stealth Mode
 Total: 9 LED



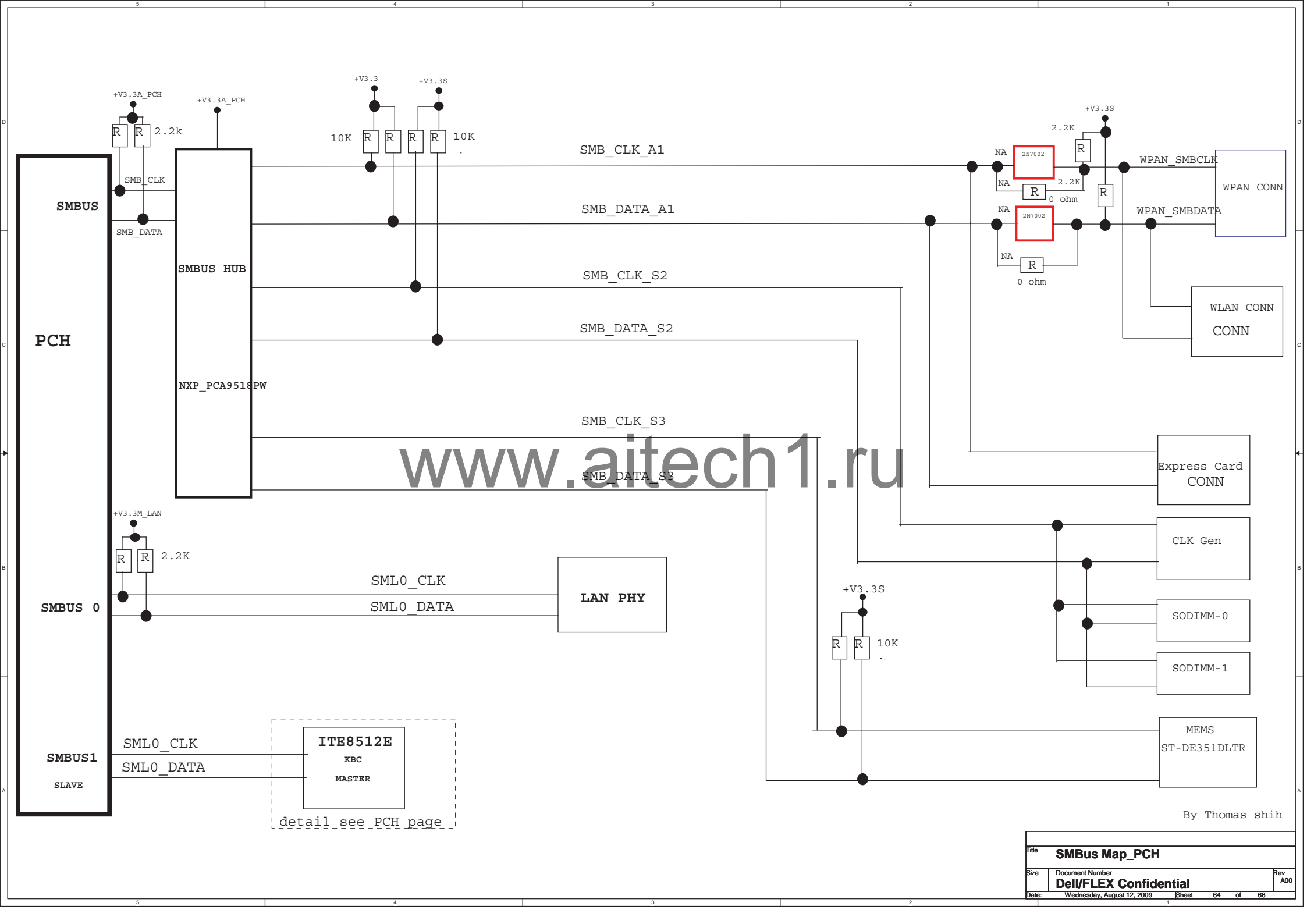
+3.3V_F347 behavior

	State			
	S0	S3	S4	S5
AC In	ON	ON	ON	ON
BAT only	ON	ON	Off	Off

Title			LED BOARD		
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KBC Powre Up Sequence

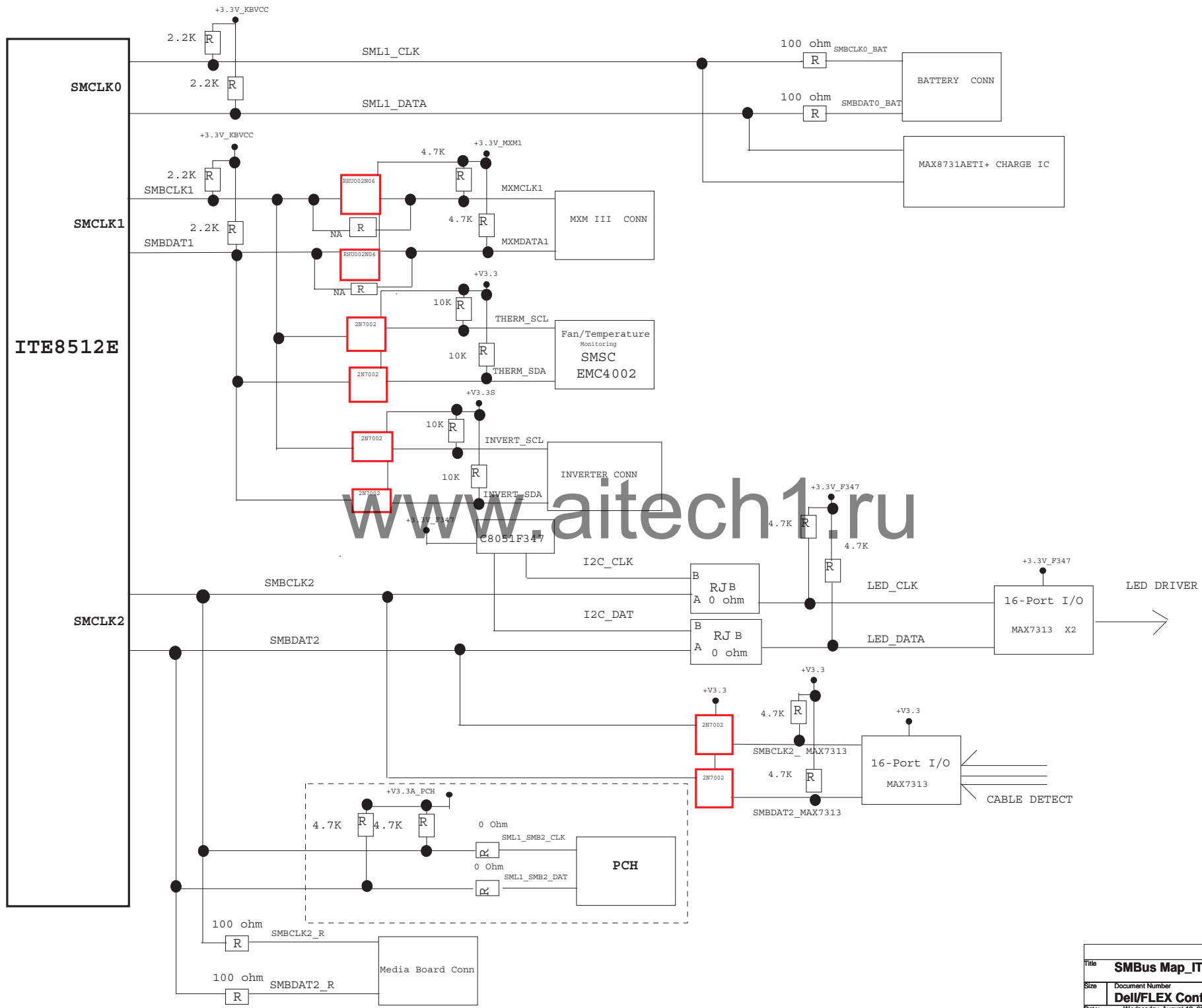




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By Thomas shih

Title		SMBus Map_PCH			
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Version change list (P.I.R. List)

EE change

EMI change POWER change

Item	Fixed Issue	Reason for Change	Rev	PG#	Modify List	B Ver#	Phase
1	CPU thermal shutdown change to 93C	6/23 PWA X120 was changed	A00	36	R752 change from 953_F to 1.33k_F ohm	A00	Safe Launch
2	FOR LOW_BAT & cost down	7/9 PWA X220 was changed	A00	18	Q37 change from mount to NA	A00	Safe Launch
3	Board ID Straps	Change for A00 version	A00	37	Change R104, R120 mount; R110, R112 NA	A00	Safe Launch
4	K/B LED grey	Increase K/B LED brightness	A00	41	R725, R701, R703, R671, R672, R705, R670, R718 change from 10 ohm to 4.7 ohm	A00	Safe Launch
5	+V0.75S leakage saving	+V0.75S leakage saving	A00	50	PR124 mount change to NA	A00	Safe Launch
6	Intel confirm to remove	Intel confirm to remove	A00	16	RJ5A, RJ6A, R362, R363, R355, R354 mount change to NA	A00	Safe Launch
7	Remove XDP function	Remove XDP function	A00	13	CN601, CN26, R651, R387, R359 Mount change to NA	A00	Safe Launch
8	Change MXM CONN footprint	Change MXM CONN footprint	A00	25	Change MXM CONN footprint and library	A00	Safe Launch
9	Remove on board power button	Only for test	A00	39	Mount change to NA: SW600.	A00	Safe Launch
10	Remove eDP function	Remove eDP function	A00	27	Mount change to NA: CN27, C817, R906, R907, R908, R909, R898, R899, R900, R901, R902, R903, C811, C812, C813, C814, C815, C816.	A00	Safe Launch
11	Change for factory without CPU test	Change for factory without CPU test	A00	52	PR9 change from 10ohm to 2Kohm	A00	Safe Launch
1	For +V1.1S_VTT feedback	For +V1.1S_VTT feedback	A00	54	PR647 NA change to mount	A00	Safe Launch
1	For USB 480Mhz over limit issue	For USB 480Mhz over limit issue	A00	28	R100, R101 change to NA. L12 change to mount.	A00	Safe Launch
2	CRT RGB Signal quality and EMI	CRT RGB Signal quality and EMI	A00	29	L4, L7, L11 change from 75ohm_BLM18BB750SN1D to 80ohm_MMZ1608D800BT. C209, C202, C194 change from 18pF to 12pF. C192, C198, C208 change from 18pF to 33pF.	A00	Safe Launch

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